AKD4665A-A
AK4665A Evaluation board Rev.1

GENERAL DESCRIPTION

AKD4665A-A is an evaluation board for the AK4665A, 20bit CODEC with built-in Input PGA and Headphone Amplifier. The AKD4665A-A can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). AKD4665A-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4665A-A --- Evaluation board for AK4665A
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **RCA connector for an external clock input**
- **10pin Header for serial control mode**

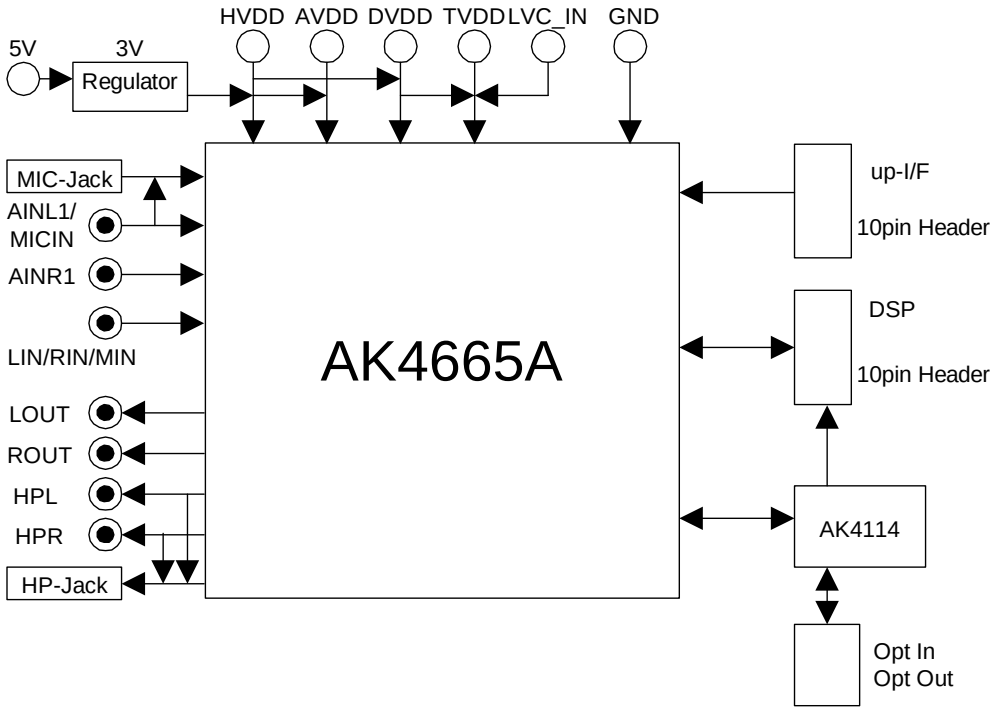


Figure 1. AKD4665A-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD, DVDD, HVDD, TVDD and LVC are supplied from the regulator. (AVDD, DVDD, HVDD, TVDD and LVC_IN jack should be open.). See "**Other jumper pins set up** (page 5)". <default>

[REG]	(red)	= 5V	
[HVDD]	(orange)	= open	: 3V is supplied to HVDD of AK4665A from regulator.
[AVDD]	(orange)	= open	: 3V is supplied to AVDD of AK4665A from regulator.
[DVDD]	(orange)	= open	: 3V is supplied to DVDD of AK4665A from regulator.
[TVDD]	(blue)	= open	: 3V is supplied to TVDD of AK4665A from regulator.
[LVC_IN]	(blue)	= open	: 3V is supplied to logic block of LVC from regulator.
[VD_IN]	(orenge)	= 2.7 ~ 3.6V	: for other logic (typ. 3V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

1-2) When AVDD, DVDD, HVDD, TVDD and LVC are not supplied from the regulator. (AVDD, DVDD, HVDD, TVDD and LVC jack should be junction.) See "**Other jumper pins set up** (page 5)".

[REG]	(red)	= "REG" jack and JP2 should be open.
[HVDD]	(orange)	= 2.6 ~ 3.6V : for HVDD of AK4665A (typ. 3V)
[AVDD]	(orange)	= 2.6 ~ 3.6V : for AVDD of AK4665A (typ. 3V)
[DVDD]	(orange)	= 2.6 ~ 3.6V : for DVDD of AK4665A (typ. 3V)
[TVDD]	(blue)	= 1.6 ~ 3.6V : for TVDD of AK4665A (typ. 3V)
[LVC_IN]	(blue)	= 1.65 ~ 5.5V: for logic block of LVC (typ. 3V)
[VD_IN]	(orenge)	= 2.7 ~ 3.6V : for other logic (typ. 3V)
[AGND]	(black)	= 0V : for analog ground
[DGND]	(black)	= 0V : for logic ground

Each supply line should be distributed from the power supply unit.
AVDD and DVDD each must be same voltage level, and TVDD and LVC_IN each too.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4665A and AK4114 should be reset once bringing SW1, 2 "L" upon power-up.

■ Evaluation mode

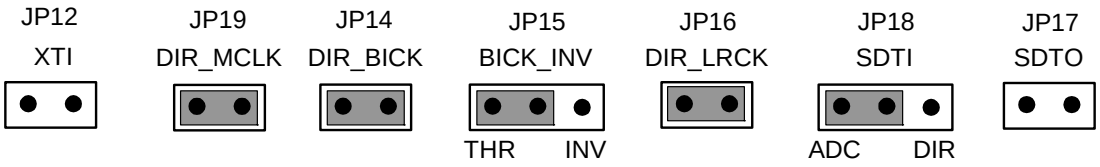
In case of AK4665A evaluation using AK4114, same audio interface format should be set for both AK4665A and AK4114. About AK4665A's audio interface format, refer to datasheet of AK4665A. About AK4114's audio interface format, refer to Table 2 in this manual.

Applicable Evaluation Mode

(1) Evaluation of loop-back mode (Default)
(2) Evaluation of using DIR of AK4114 (opt-connector)
(3) Evaluation of using DIT of AK4114 (opt-connector)
(4) All interface signals including master clock are fed externally.

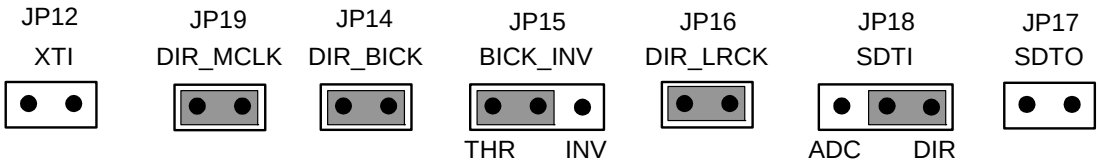
(1) Evaluation of loop-back mode (Default)

Nothing should be connected to PORT3. PORT1(TORX141), or X'tal mode of the AK4114 is used.
When an external clock through an RCA connector (J10: MCLK) is supplied, short JP12 (XTI). JP13 (EXT) and R28 should be properly selected in order to much the output impedance of the clock generator. Then X'tal(X1) and capacitance (C35,C36) should be removed.



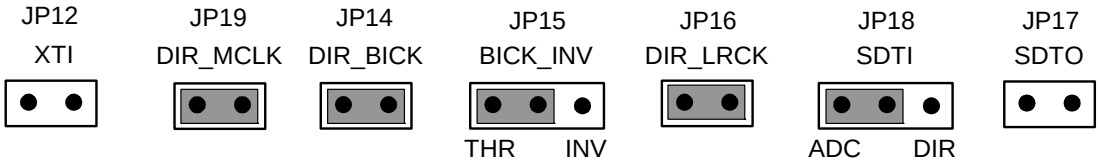
(2) Evaluation of using DIR of AK4114 (opt-connector)

PORT1(TORX141), is used. DIR generates MCLK, BICK, LRCK and SDTI from the received data through optical connector (TORX141). Used for the evaluation using CD test disk. Nothing should be connected to PORT3.



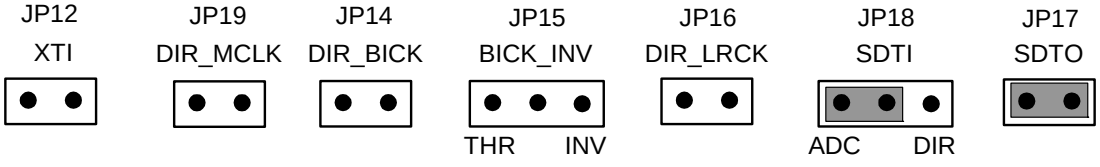
(3) Evaluation of using DIT of AK4114 (opt-connector)

PORT1(TORX141) and PORT2(TOTX141), or X'tal mode of the AK4114 and PORT2(TOTX141) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input.
Nothing should be connected to PORT3.
When an external clock through a RCA connector (J10: MCLK) is supplied, short JP12 (XTI). JP13 (EXT) and R28 should be properly selected in order to much the output impedance of the clock generator. Then X'tal(X1) and capacitance (C35,C36) should be removed.



(4) All interface signals including master clock are fed externally.

When all interface signals through PORT3 are supplied, the jumper pins should be set to the following.



■ DIP Switch set up

[SW2] (MODE) : Mode Setting of AK4114
ON is "H", OFF is "L".

No.	Name	Default	ON ("H")	OFF ("L")
1	DIF0	OFF	AK4114 Audio Format Setting See Table 2	
2	DIF1	OFF		
3	DIF2	ON		
4	CM0	OFF	Clock Operation Mode select See Table 3	
5	OCKS1	OFF	Master Clock Frequency Select See Table 4	

Table 1. Mode Setting for AK4114

Mode	Setting for AK4114 Audio Interface Format					Register setting for AK4665A Audio Interface Format		
	DIF2	DIF1	DIF0	DAUX	SDTO	DIF1	DIF0	
0	0	0	0	24bit, Left justified	16bit, Right justified	0	0	
2	0	1	0	24bit, Left justified	20bit, Right justified	0	1	
4	1	0	0	24bit, Left justified	24bit, Left justified	1	0	Default
5	1	0	1	24bit, I^2S	24bit, I^2S	1	1	

Table 2. Setting for AK4114 Audio Interface Format

SW2-#4 (CM0)	Clock Mode	Clock source	SDTO	
OFF	PLL Mode	PORT1 (TORX141)	RX (Optical)	Default
ON	X'tal Mode	X1 (X'tal) or J10 (RCA)	DAUX (ADC)	

Table 3. Clock Operation Mode select

SW2-#5 (OCKS1)	PLL Mode	X'tal Mode	
OFF	256fs	256fs	Default
ON	512fs	512fs	

Table 4. Master Clock Frequency Select

■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   OPEN : Separated.
   SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP3 (REG) : HVDD of the AK4665A
   OPEN : HVDD is supplied from "HVDD " jack.
   SHORT : HVDD is supplied from the regulator ("HVDD" jack should be open). < Default >

3. JP3 (AVDD_SEL) : AVDD of the AK4665A
   OPEN : AVDD is supplied from "AVDD " jack.
   SHORT : AVDD is supplied from "HVDD" ("AVDD" jack should be open). < Default >

4. JP4 (DVDD_SEL) : DVDD of the AK4665A
   OPEN : DVDD is supplied from "DVDD " jack. < Default >
   SHORT : DVDD is supplied from "HVDD" ("DVDD" jack should be open).

5. JP6 (TVDD_SEL), JP7 (LVC_SEL):

JP6	JP7	TVDD is supplied from	Logic block of LVC is supplied from	Note	
OPEN	OPEN	"TVDD" jack	"LVC_IN" jack	-	
OPEN	TVDD	"TVDD" jack	"TVDD" jack	"LVC_IN" jack should be open.	
OPEN	VD	"TVDD" jack	"VD_IN" jack	"LVC_IN" jack should be open.	
SHORT	OPEN	"DVDD"	"LVC_IN" jack	"TVDD" jack should be open.	
SHORT	TVDD	"DVDD"	"TVDD"	"TVDD" and "LVC_IN" jack should be open.	<Default>
SHORT	VD	"DVDD"	"VD" jack	TVDD" and "LVC_IN" jack should be open.	

Table 5. JP6 (TVDD_SEL), JP7 (LVC_SEL) select

6. JP5 (MPWR) : Connection between MPWR pin and MICIN pin of the AK4665A
   OPEN : MPWR is not connected to MICIN.
   SHORT : MPWR is connected to MICIN. < Default >

■ The function of the toggle SW

[SW1] (DIR) : Power control of AK4114. Keep “H” during normal operation.
Keep “L” when AK4114 is not used.

[SW3] (PDN) : Power control of AK4665A. Keep “H” during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4665A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4665A-A

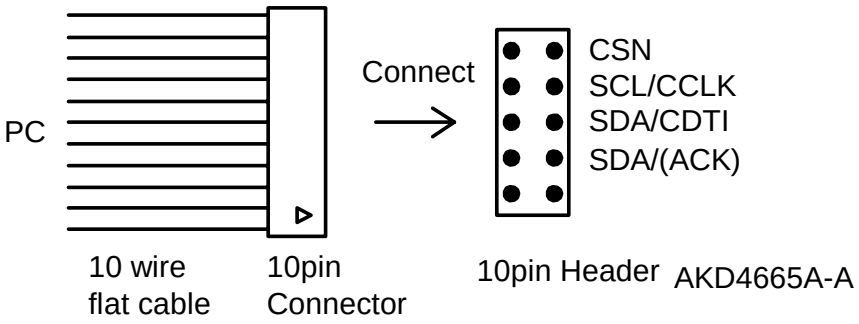


Figure 2. Connect of 10 wire flat cable

■ Analog Input / Output Circuits

(1) Input Circuits

a) MIC/AINL1/AINR1 Input Circuit

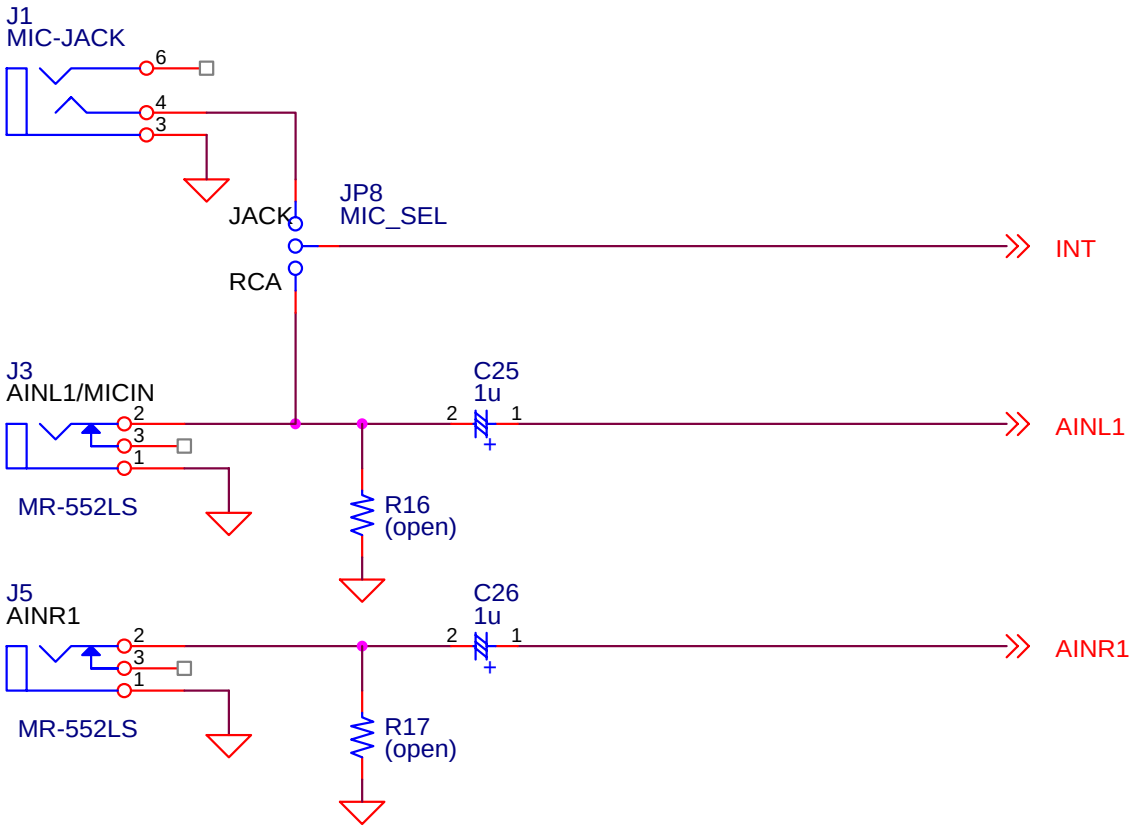
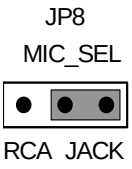
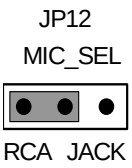


Figure 3. MIC/AINL1/AINR1 Input Circuit

(a-1) Analog signal is input to MICIN pin via J1 (MIC-JACK) connector.



(a-2) Analog signal is input to MICIN pin via J3 (AINL1/MICIN) connector.



b) LIN/RIN/MIN Input Circuit

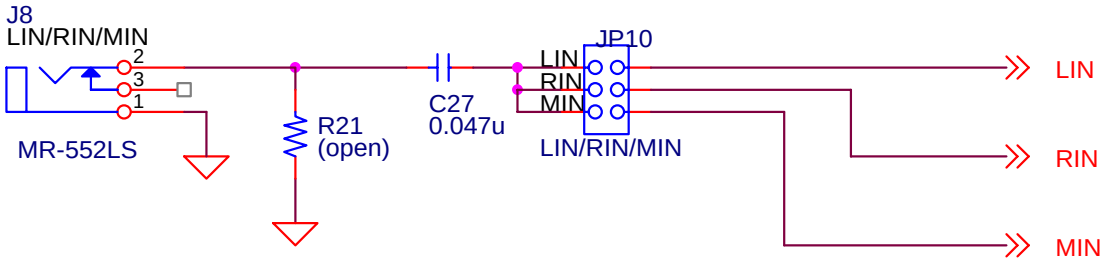


Figure 4. LIN/RIN/MIN Input Circuit

(2) Output Circuits

a) LOUT/ROUT Output Circuit

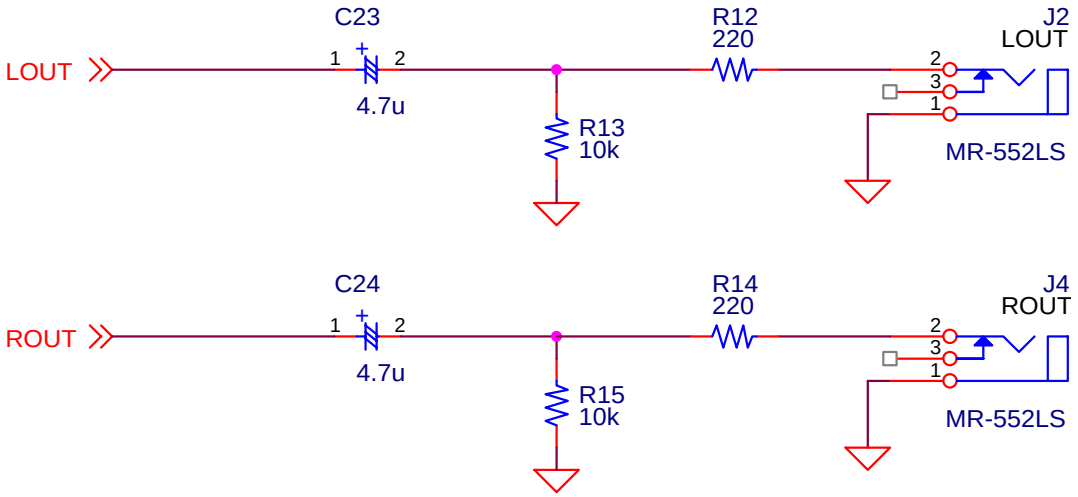


Figure 5. LOUT/ROUT Output Circuit

b) HPL/HPR Output Circuit

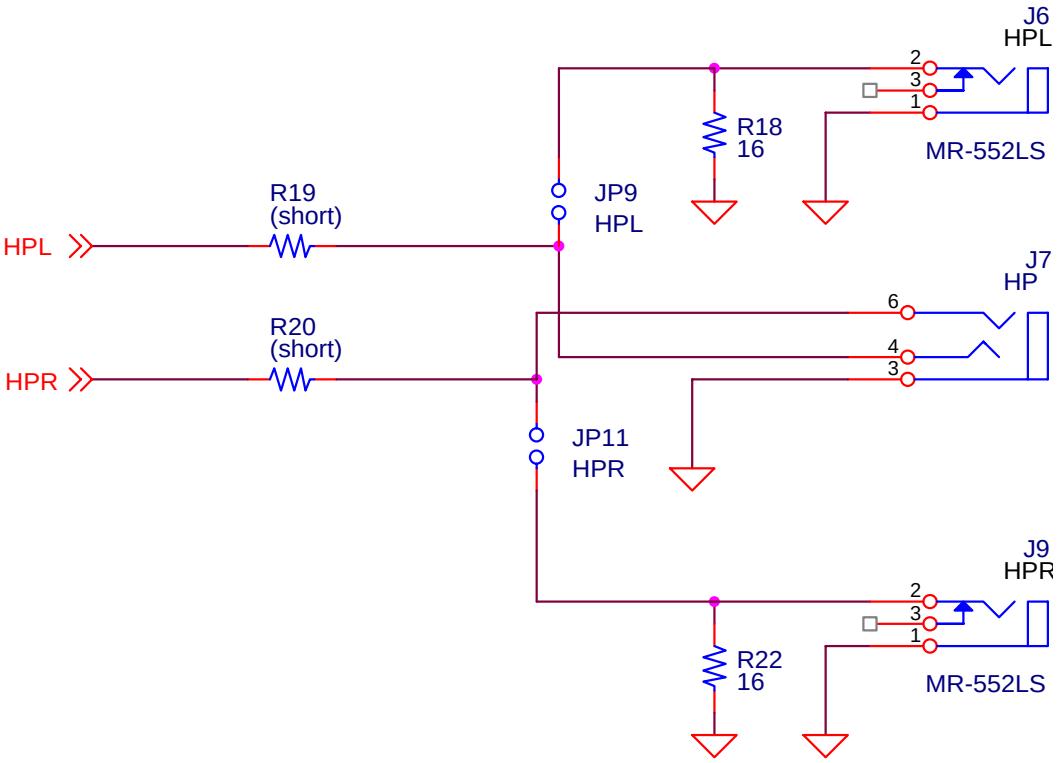
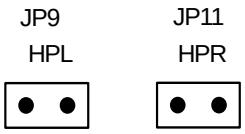
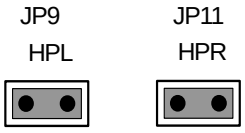


Figure 6. HPL/HPR Output Circuit

(b-1) HPL and HPR pins are outputted from J7 (mini jack).



(b-2) HPL and HPR pins are outputted from J6 and J9.



∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

2. Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4665A-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4665A-A by 10-line type flat cable (packed with AKD4665A-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AKD4665A-A Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4665a-a.exe” to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.
3. Click “Write default” button

■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default] : Initialize the register of the AK4665A.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to write data by keyboard operation.
6. [Function3] : The sequence of register setting can be set and executed.
7. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE] : Save the current register setting.
10. [OPEN] : Write the saved values to all register.
11. [Write] : Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to the AK4665A, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4665A, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate DATT

There are dialogs corresponding to register of 05h, 0Ah, 0Bh and 0Ch.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to the AK4665A by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4665A, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is “akr”.

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is “akr”.

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4665A. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is “aks”.

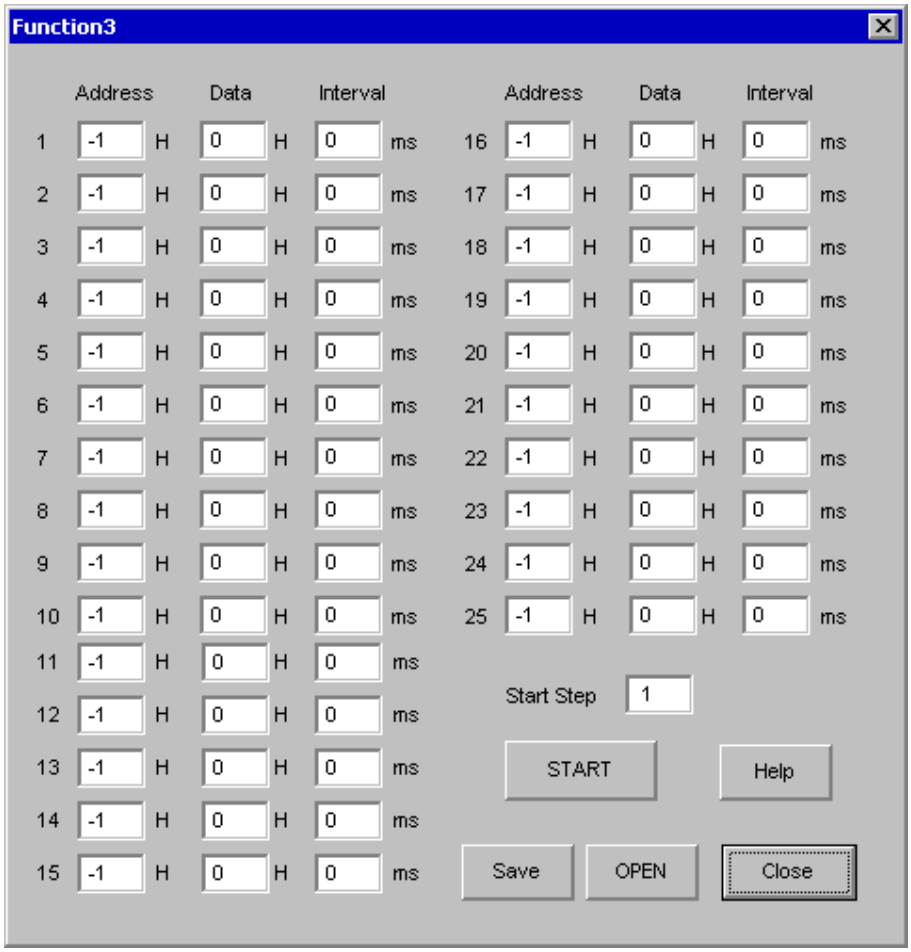


Figure 7. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 8 opens.

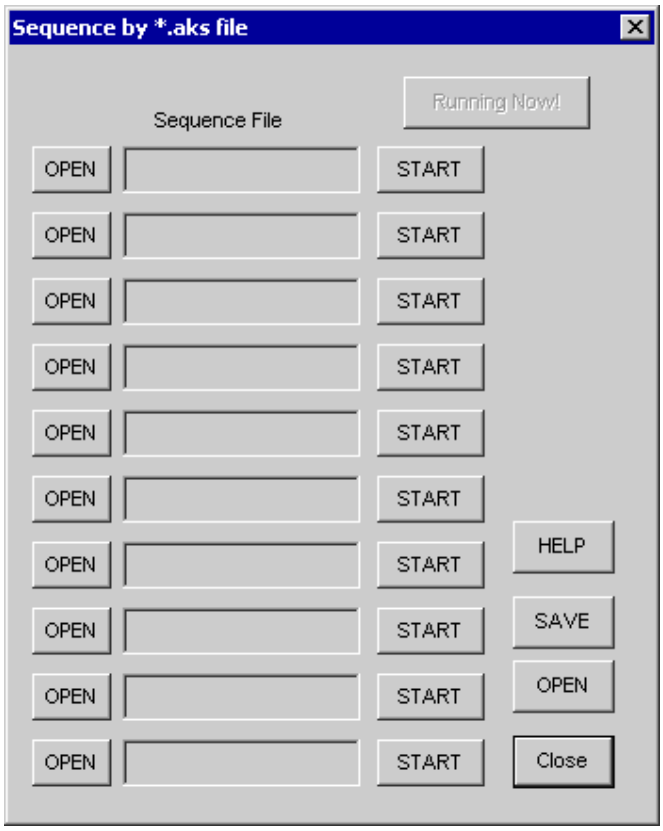


Figure 8. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 9. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

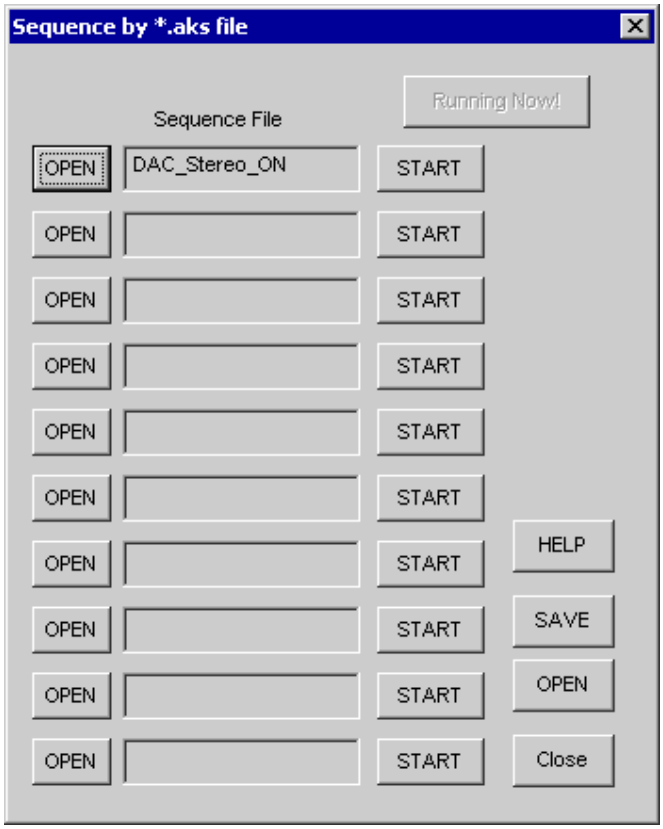


Figure 9. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 10 opens.

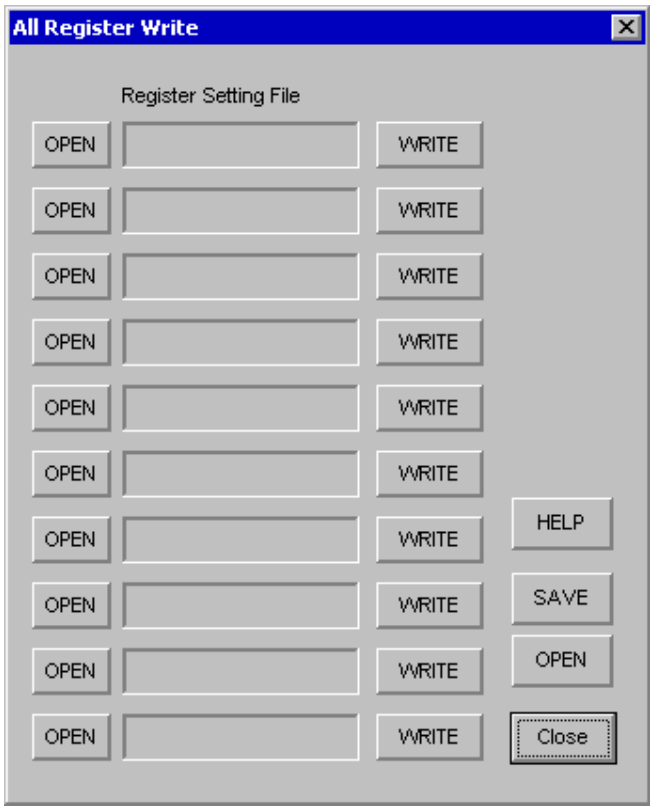


Figure 10. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 11. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

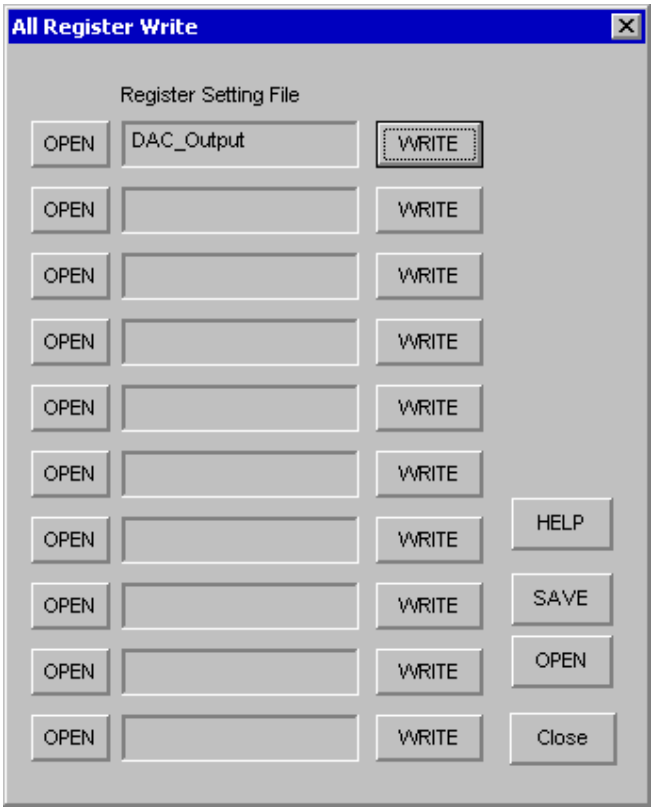


Figure 11. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precession System Two Cascade
- MCLK : 11.2896MHz
- BICK : 64fs
- fs : 44.1kHz
- Bit : 20bit
- Power Supply : AVDD = DVDD = HVDD = TVDD = 3.0V
- Measurement Filter : 10Hz ~ 20kHz
- Temperature : Room

Parameter		Result (Lch / Rch)	Unit
MIC-Amp: (MICIN pin → ADC)			
THD+N	(-1dBFS Output)	-90.6 / -90.4	dB
D-Range	(-60dB Output, A-weighted)	93.4 / 93.4	dB
S/N	(A-weighted)	93.4 / 93.4	dB

Parameter		Result (Lch / Rch)	Unit
Analog Input Characteristics: (AINL1/AINR1 pins → ADC → IVOL), IVOL=0dB, ALC1= OFF			
THD+N	(-1dBFS Output)	-91.6 / -91.2	dB
D-Range	(-60dB Output, A-weighted)	94.5 / 94.5	dB
S/N	(A-weighted)	94.6 / 94.6	dB

Parameter		Result (Lch / Rch)	Unit
Headphone-Amp: (DAC → HPL/HPR pins), RL=16Ω, HPG bit = "0", ATTL7-0=ATTR7-0 bits=0dB			
THD+N	(0dBFS Output)	-58.7 / -58.7	dB
D-Range	(-60dB Output, A-weighted)	88.4 / 88.2	dB
S/N	(A-weighted)	88.5 / 88.2	dB

Parameter		Result (Lch / Rch)	Unit
Stereo Line Output: (DAC → LOUT/ROUT pins), ATTL7-0 = ATTR7-0 = ATTS3-0 bits = 0dB			
THD+N	(0dBFS Output)	-84.5 / -84.1	dB
D-Range	(-60dB Output, A-weighted)	88.7 / 88.4	dB
S/N	(A-weighted)	88.8 / 88.5	dB

PLOT DATA

1.ADC (AINL1/AINR1 → ADC) PLOT DATA

AKM AKD4665 ADC(mic) THD+N vs.Input Level (fs=44.1kHz, fin=1kHz)

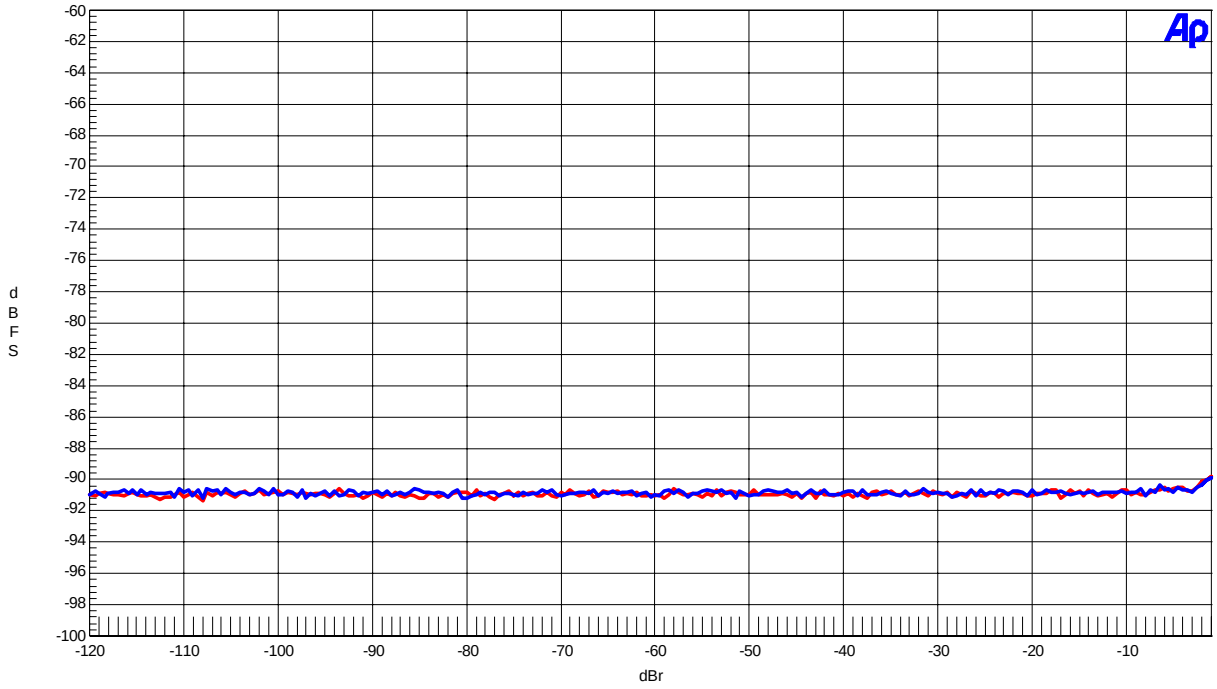


Figure 12. THD+N vs. Input Level

AKM AK4665 ADC(AIN) THD+N vs. Input Frequency (fs=44.1kHz, Input=-1dB)

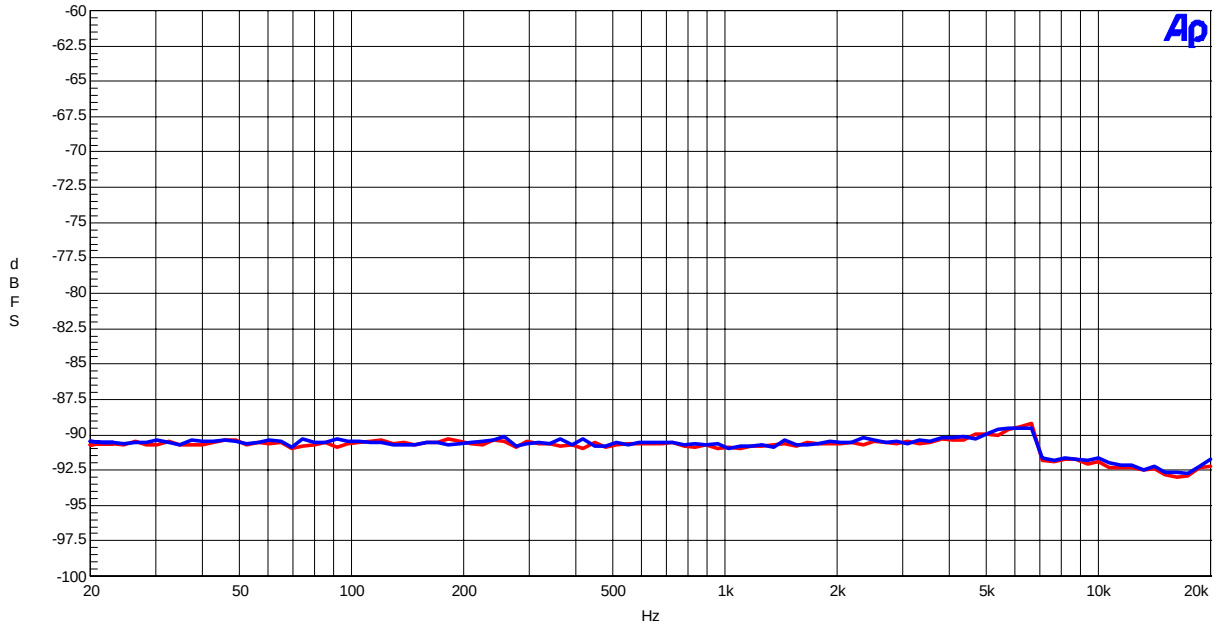


Figure 13. THD+N vs. Input Frequency (Input Level = -1dBFS)

AKM AK4665 ADC(AIN) Linearity (fs=44.1kHz, fin=1kHz)

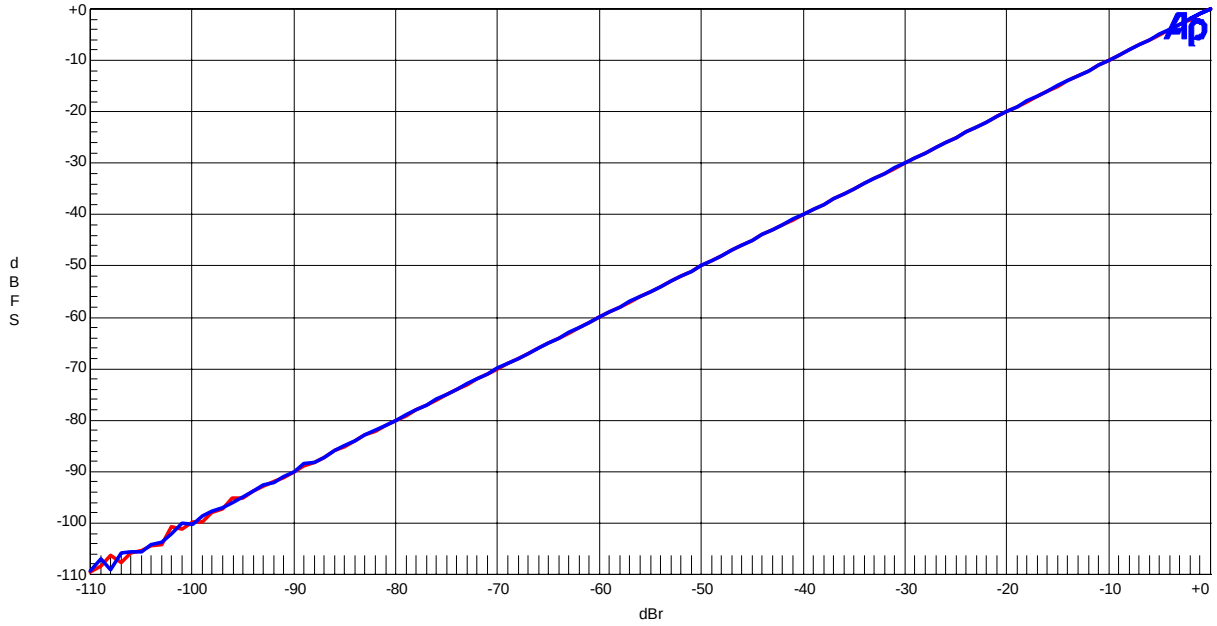


Figure 14. Linearity

AKM AK4665 ADC(AIN) Frequency Response (fs=44.1kHz, Input=-1dB)

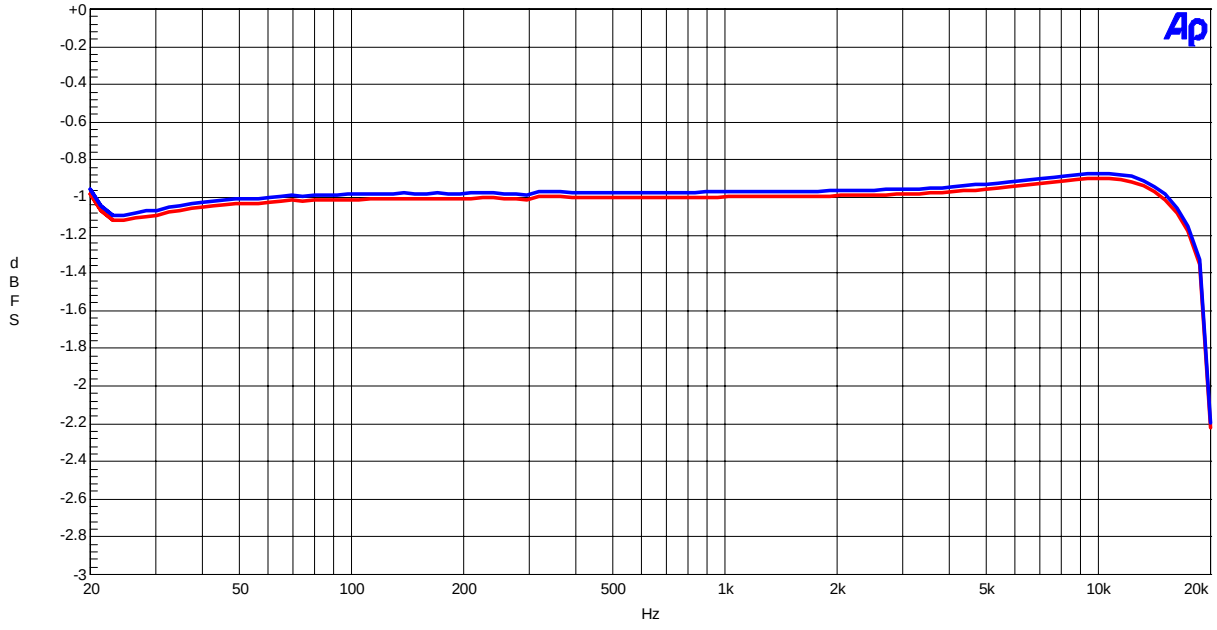


Figure 15. Frequency Response

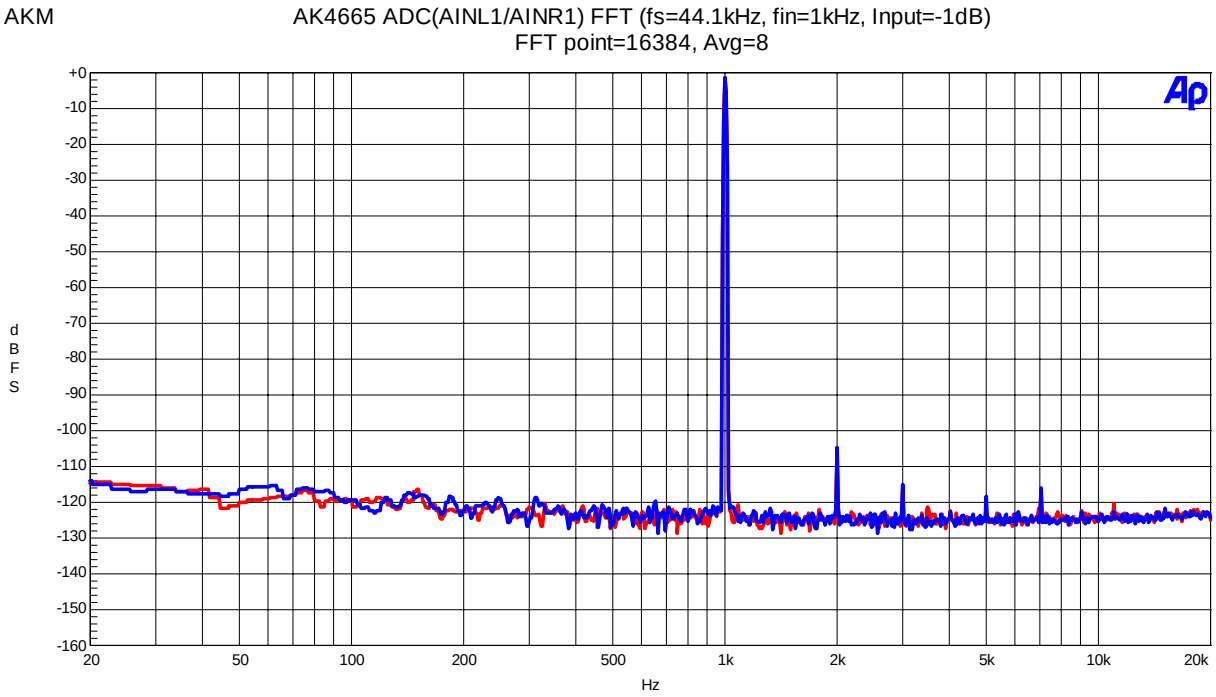


Figure 16. FFT Plot (Input level=-1dBFS)

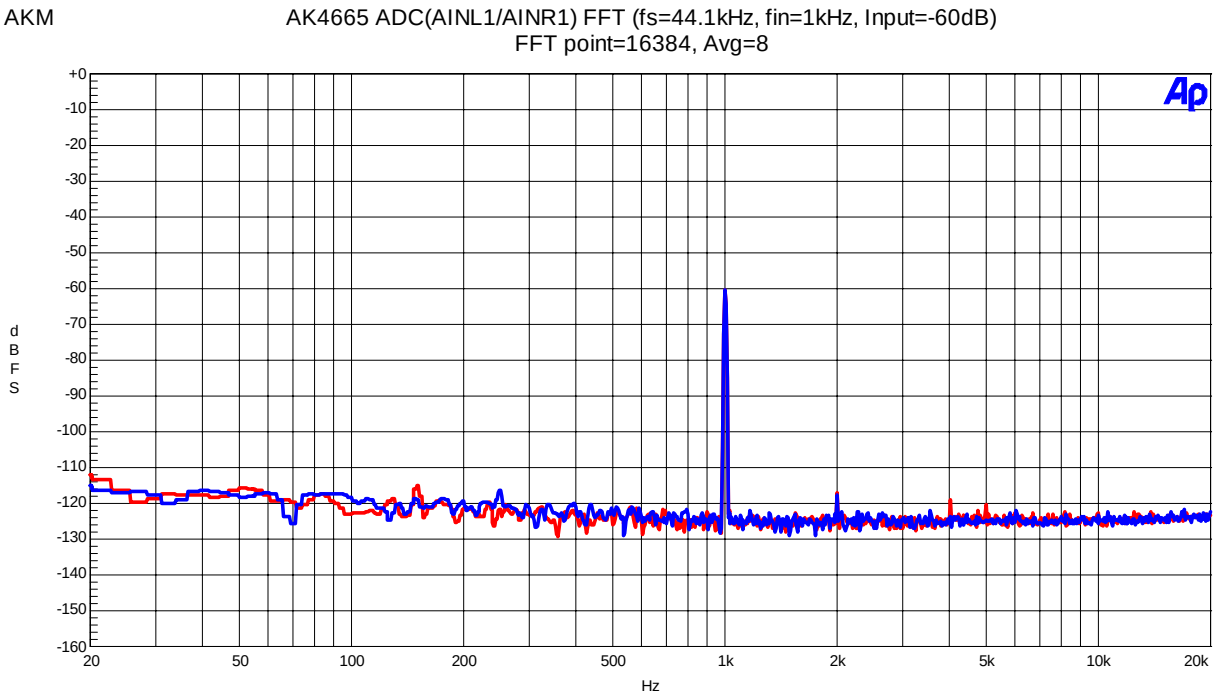


Figure 17. FFT Plot (Input level=-60dBFS)

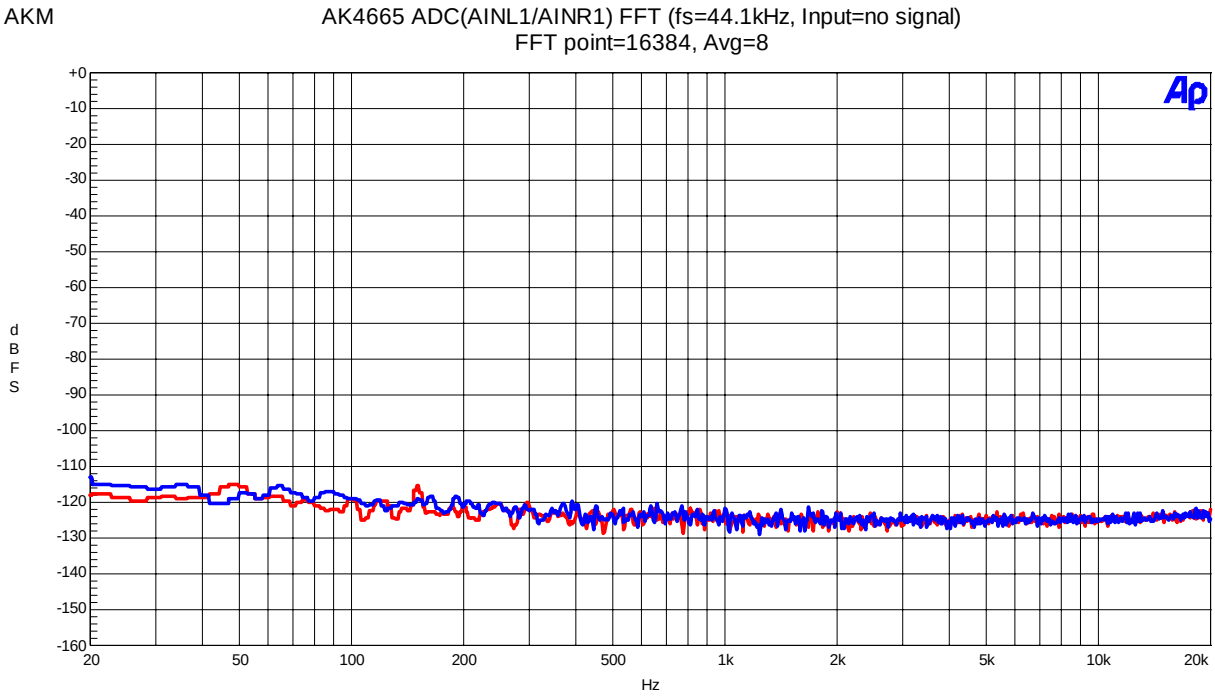


Figure 18. FFT Plot (no signal input)

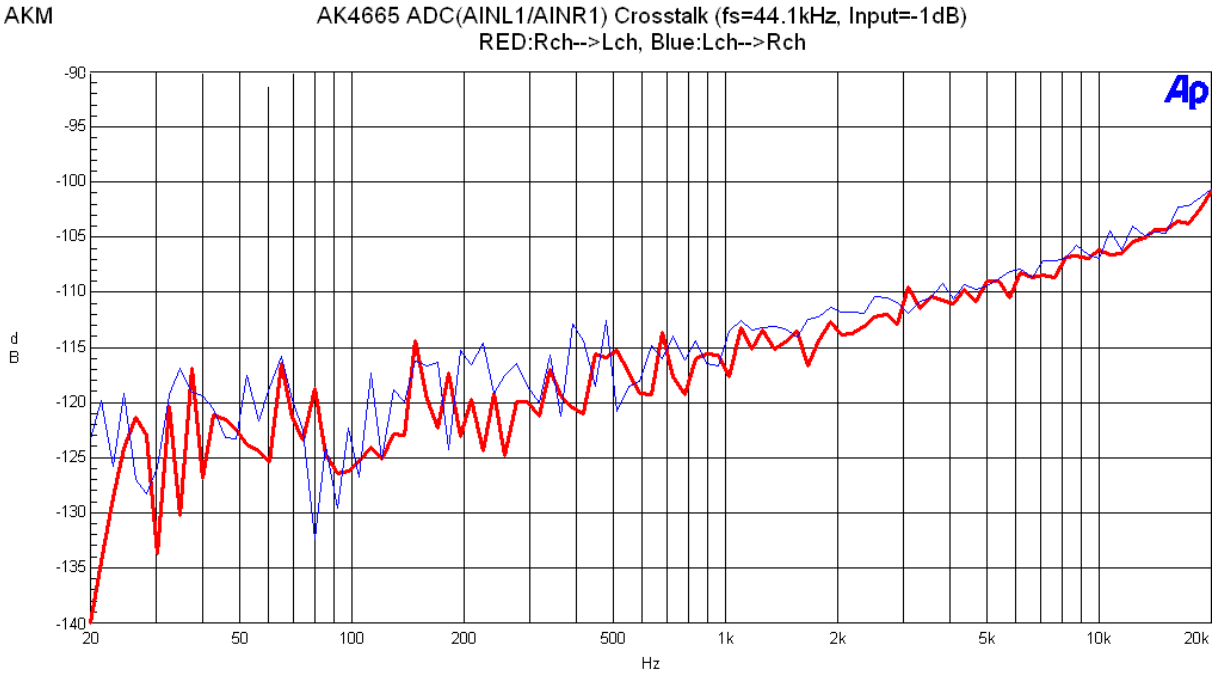


Figure 19. Crosstalk

2. DAC (DAC → LOUT/ROUT) PLOT DATA

AKM AK4665 DAC(LINEOUT) THD+N vs.Input Level (fs=44.1kHz, input=0dB)

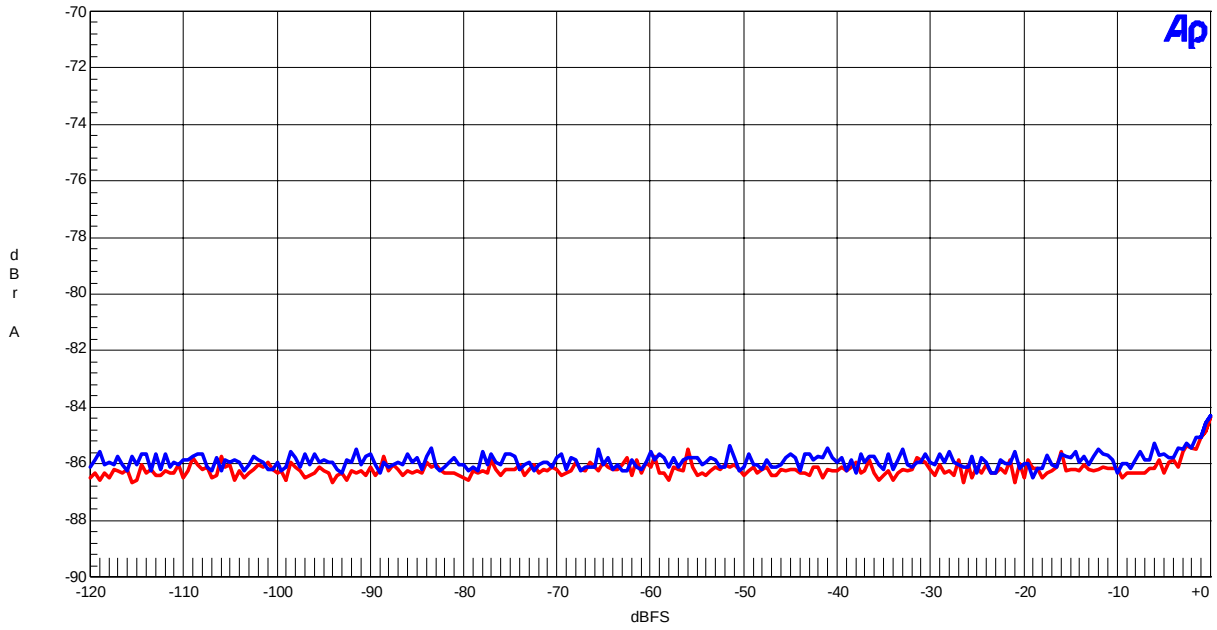


Figure 20. THD+N vs. Input Level

AKM AK4665 DAC(LINEOUT) THD+N vs.Input Frequency(fs=44.1kHz, input=0dB)

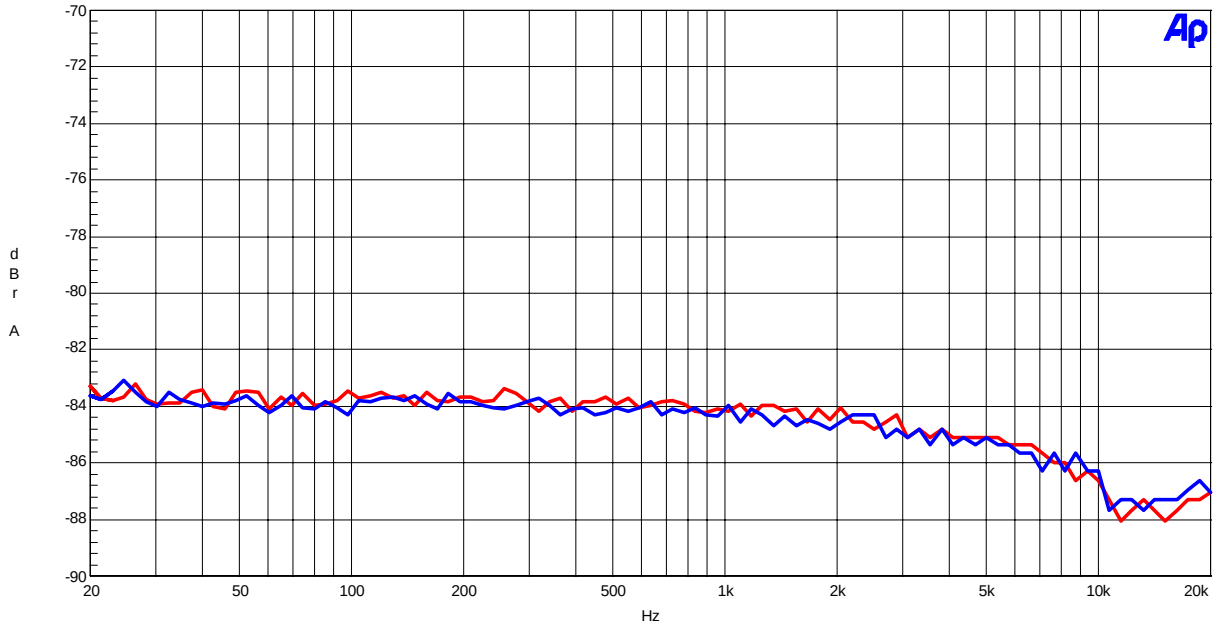


Figure 21. THD+N vs. Input Frequency (Input Level = 0dBFS)

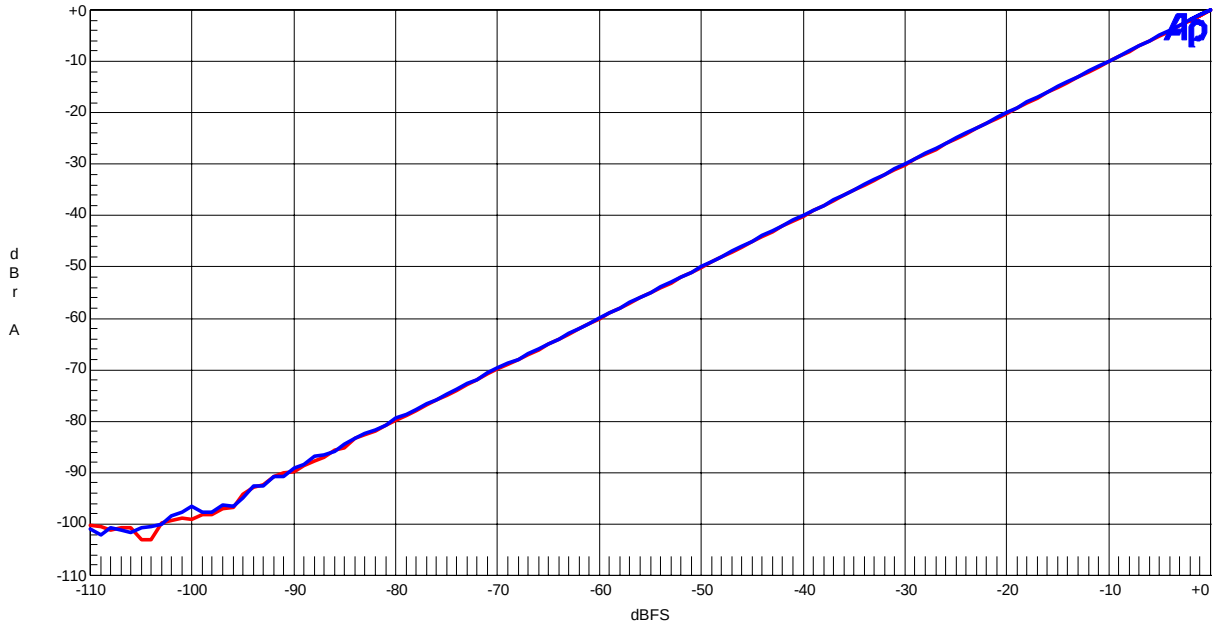


Figure 22. Linearity

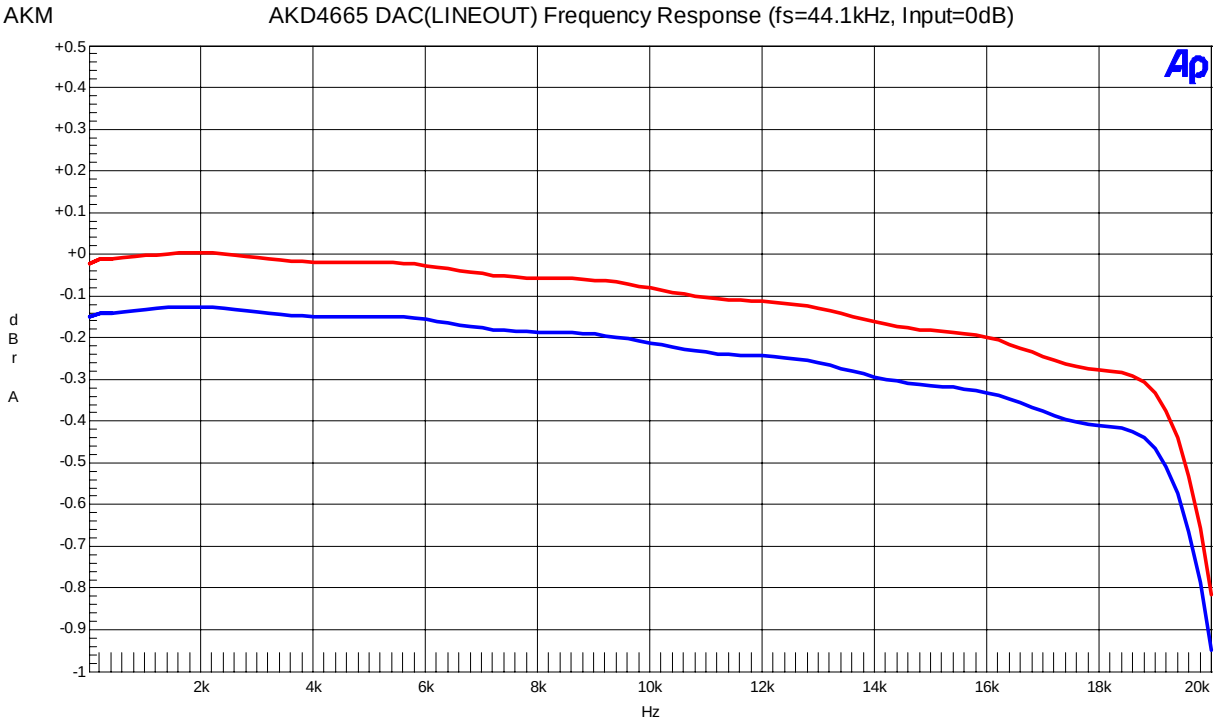


Figure 23. Frequency Response

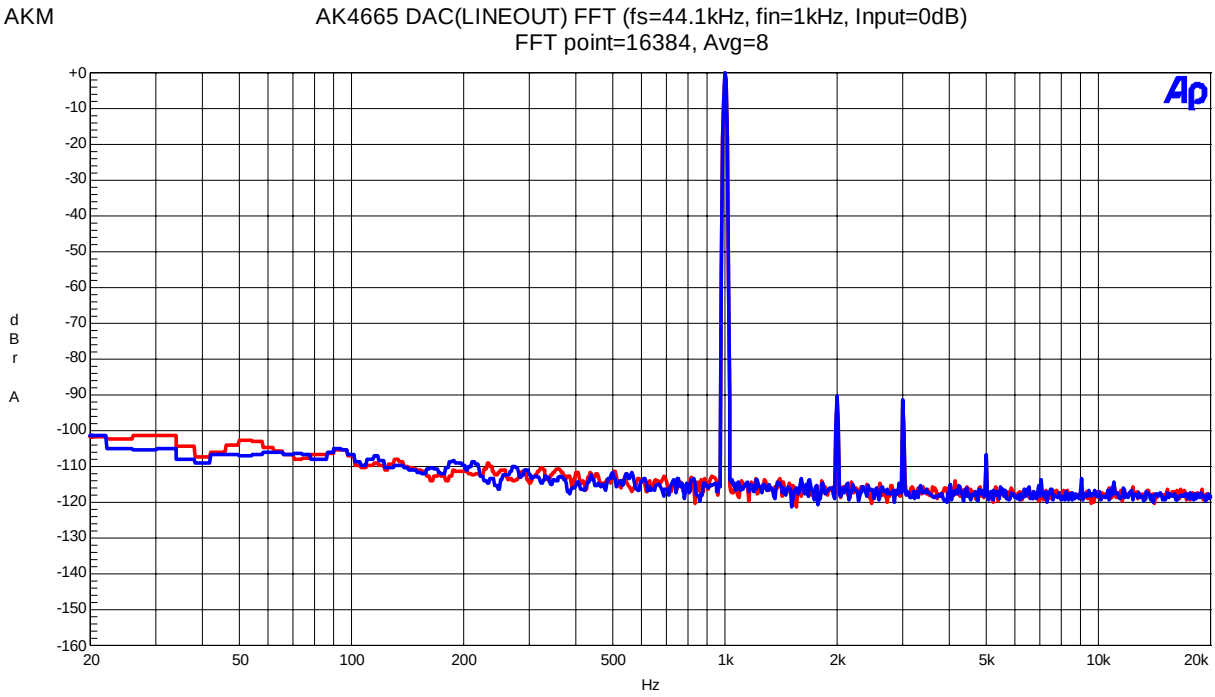


Figure 24. FFT Plot (Input level=0dBFS)

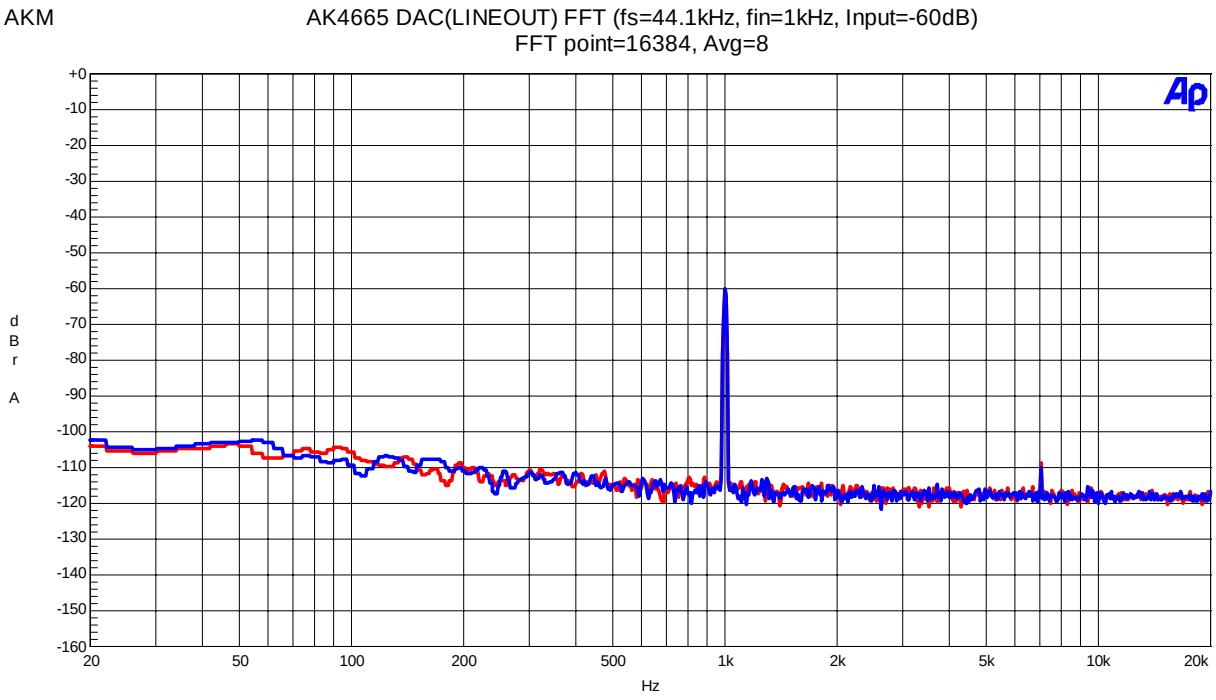


Figure 25. FFT Plot (Input level=-60dBFS)

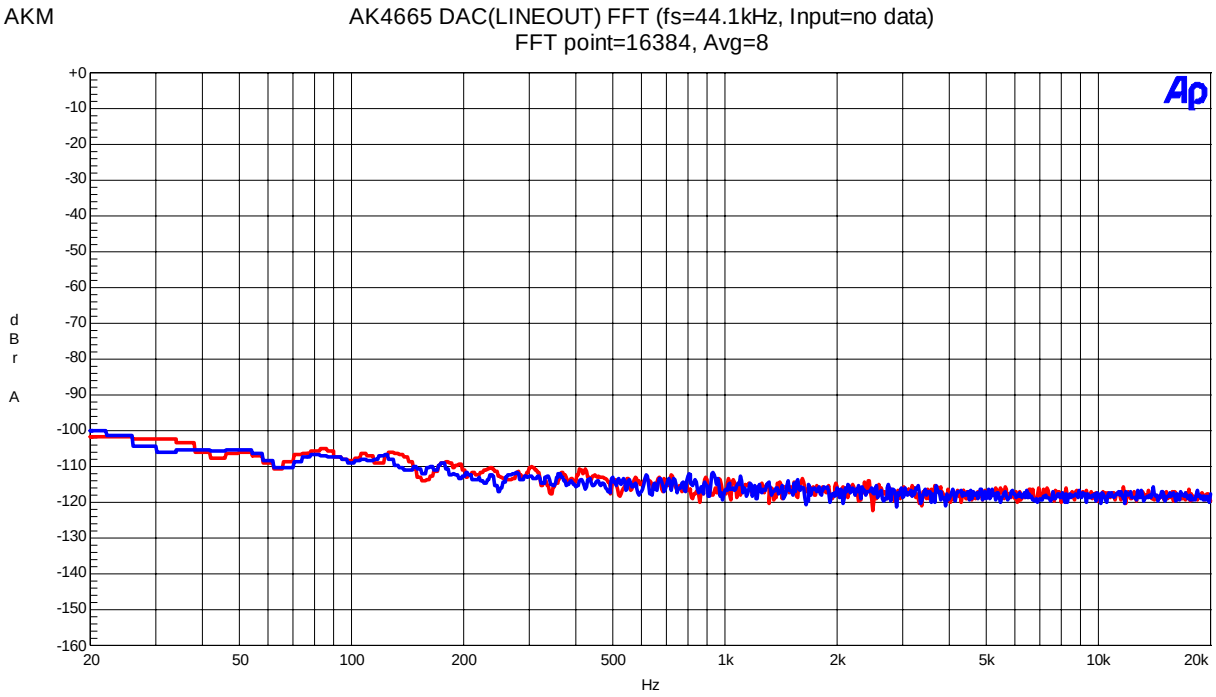


Figure 26. FFT Plot (no data input)

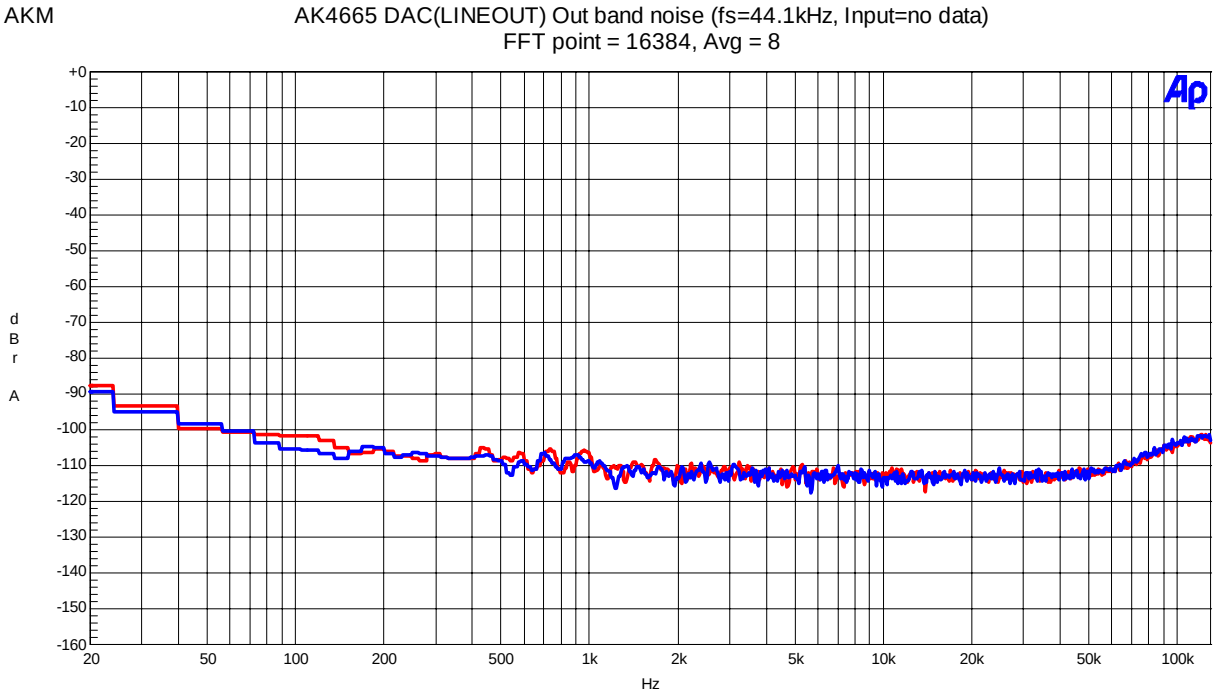


Figure 27. Out band noise (no data input)

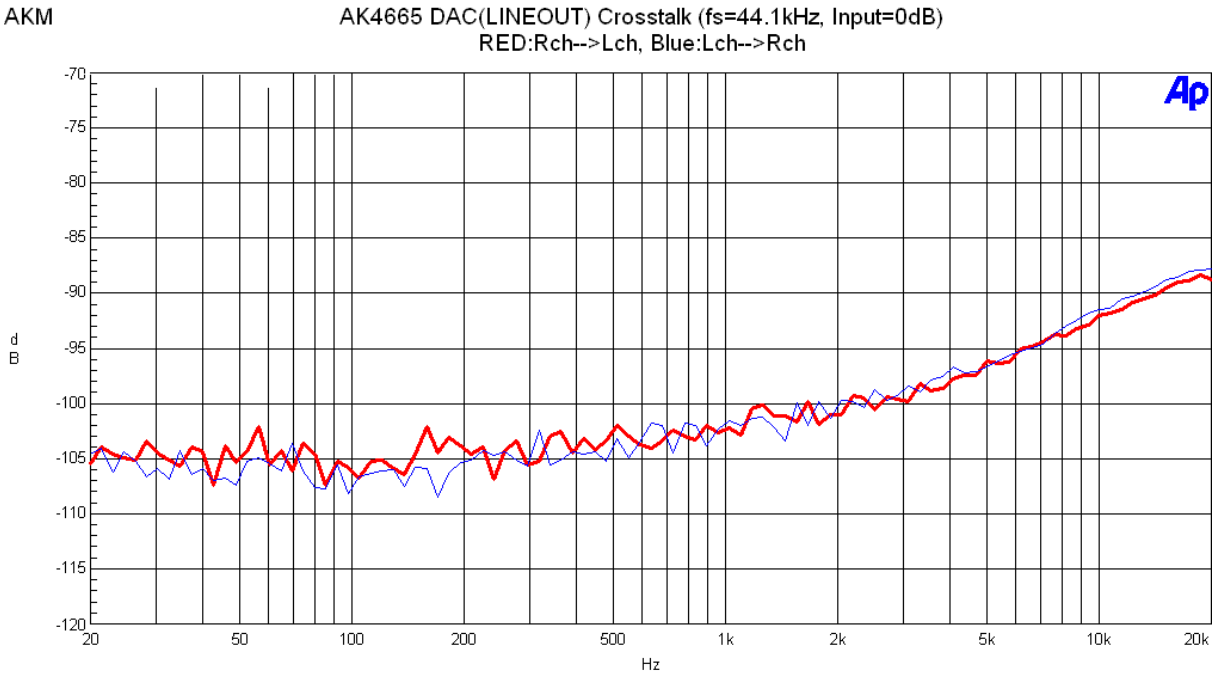


Figure 28. Crosstalk

3. DAC (DAC → HPL/HPR) PLOT DATA

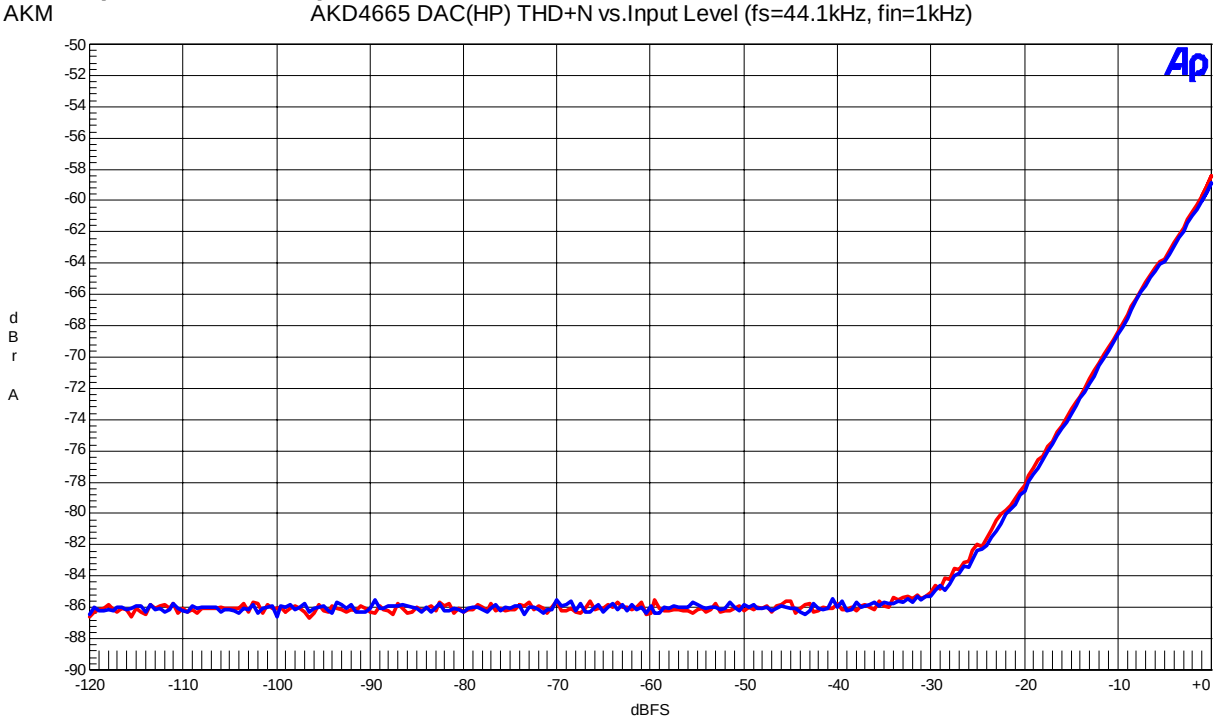


Figure 29. THD+N vs. Input Level

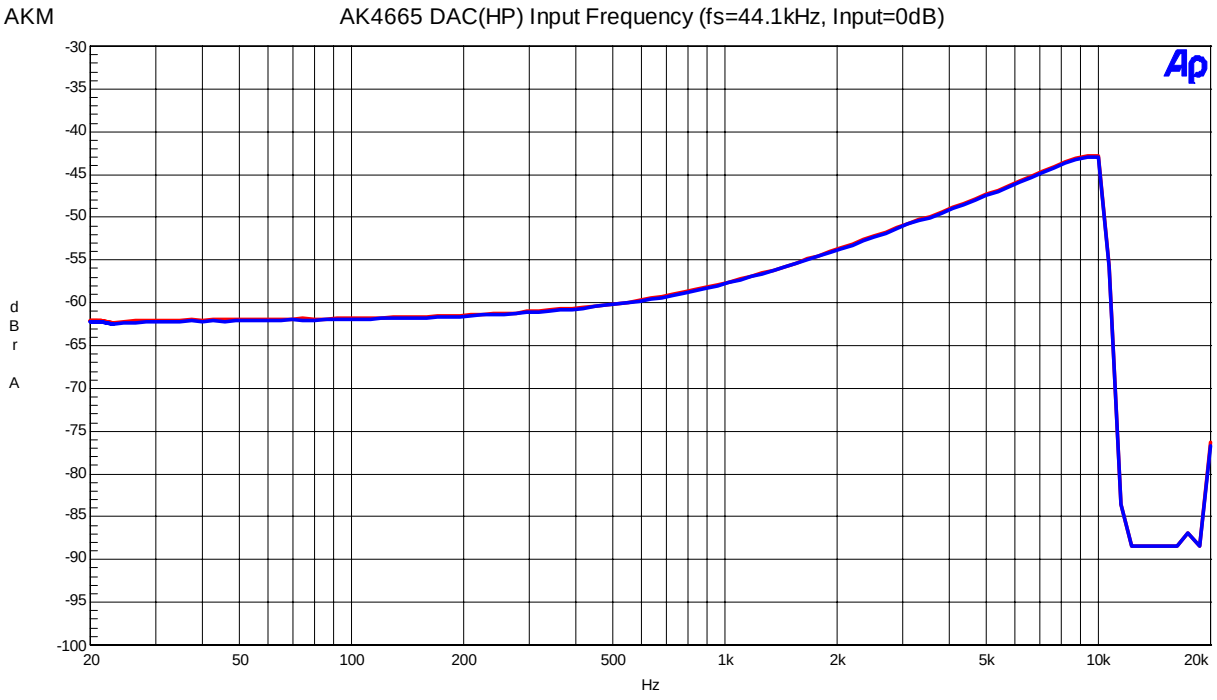


Figure 30. THD+N vs. Input Frequency (Input Level = 0dBFS)

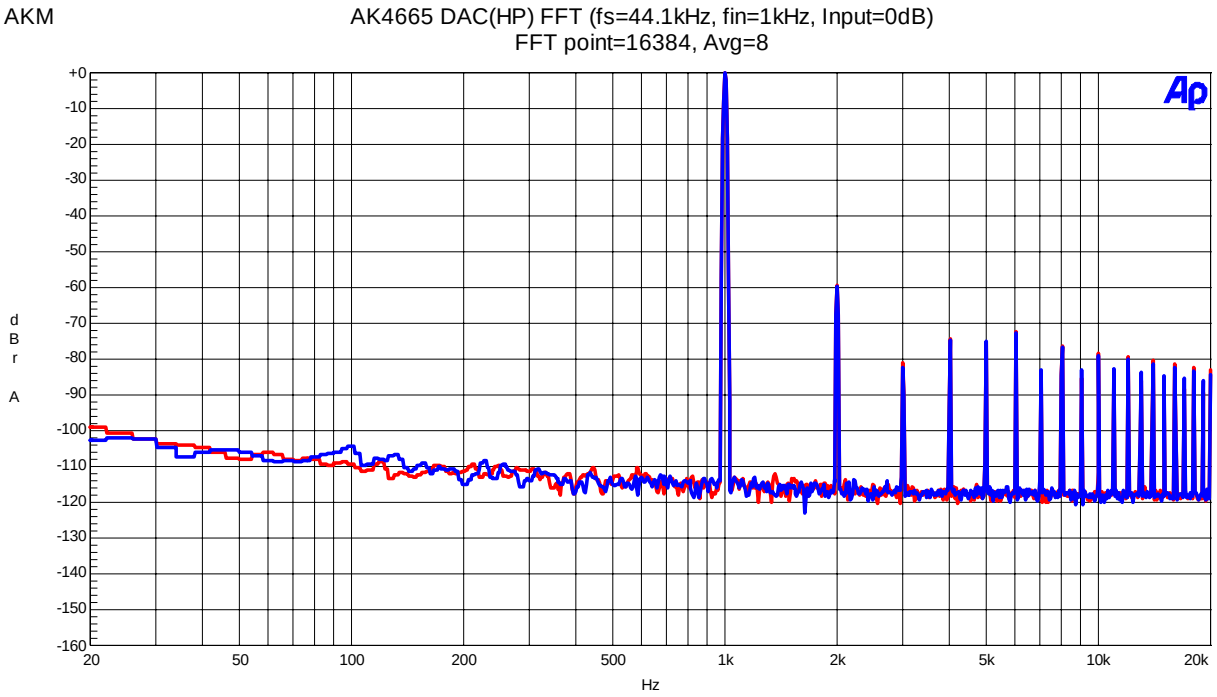


Figure 31. FFT Plot (Input level=0dBFS)

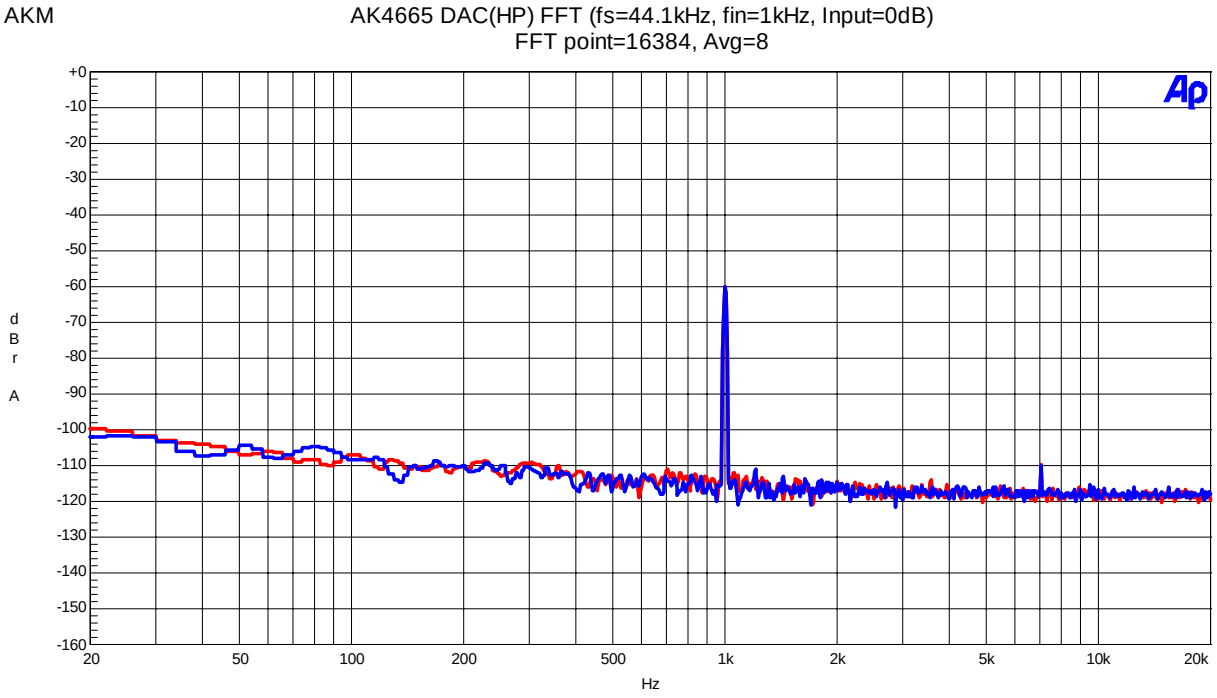


Figure 32. FFT Plot (Input level=-60.0dBFS)

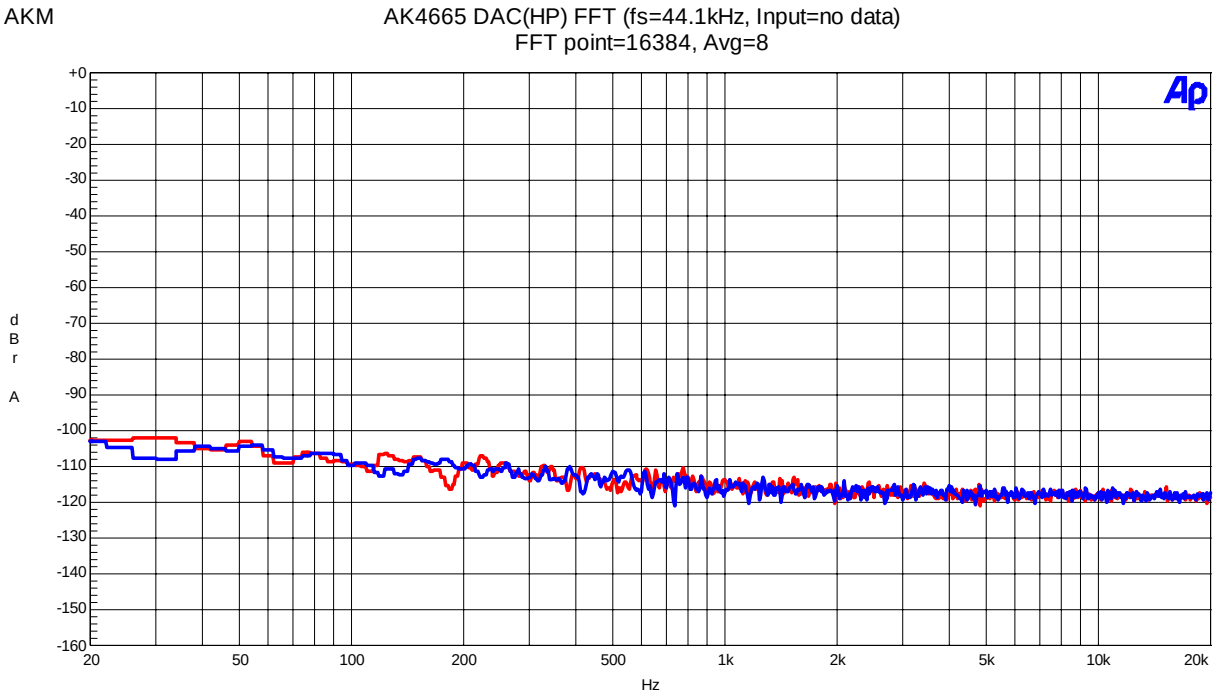


Figure 33. FFT Plot (no data input)

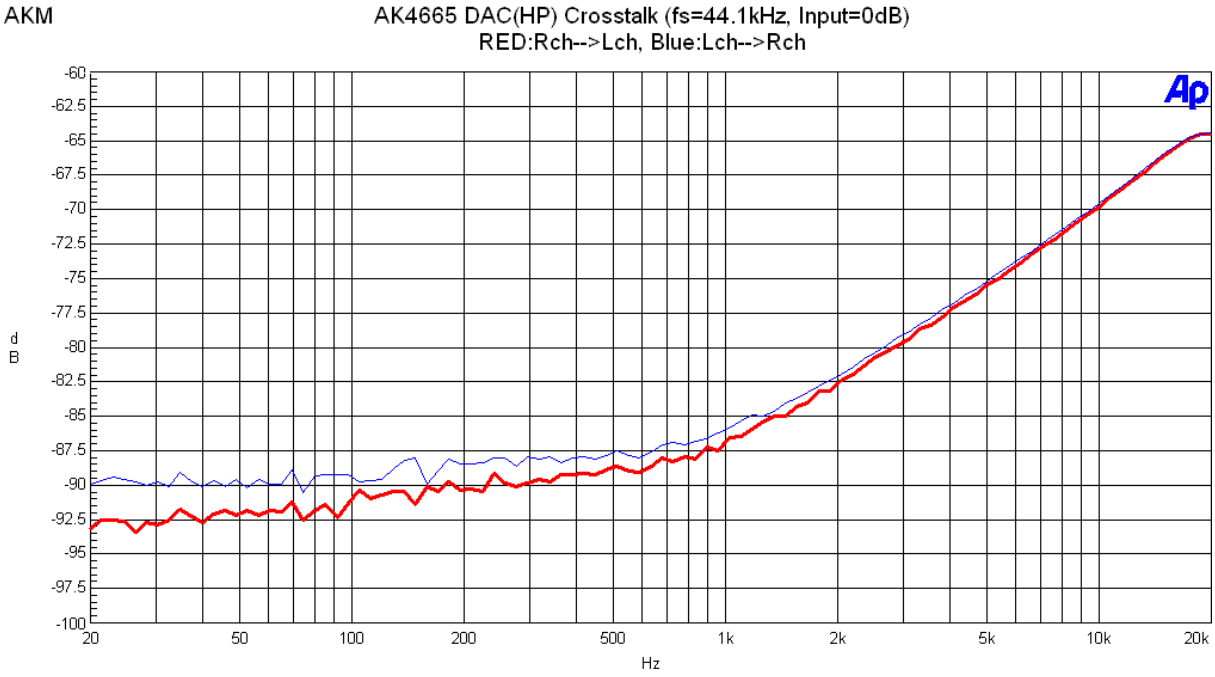
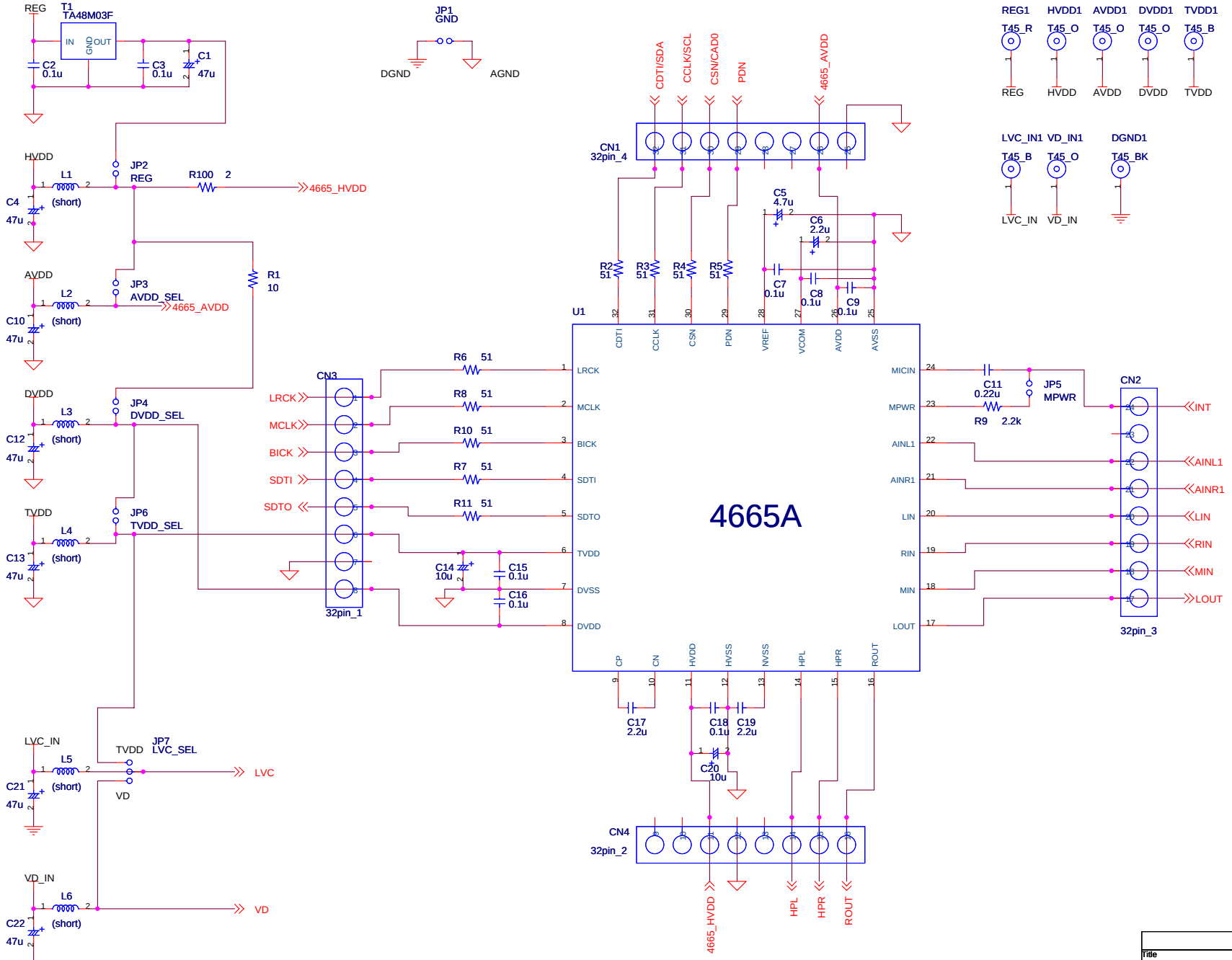


Figure 34. Crosstalk

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/12/19	KM082200	0	First Edition	
06/05/17	KM082201	1	Circuit change	A 2Ω resistor was inserted at HVDD line in series.



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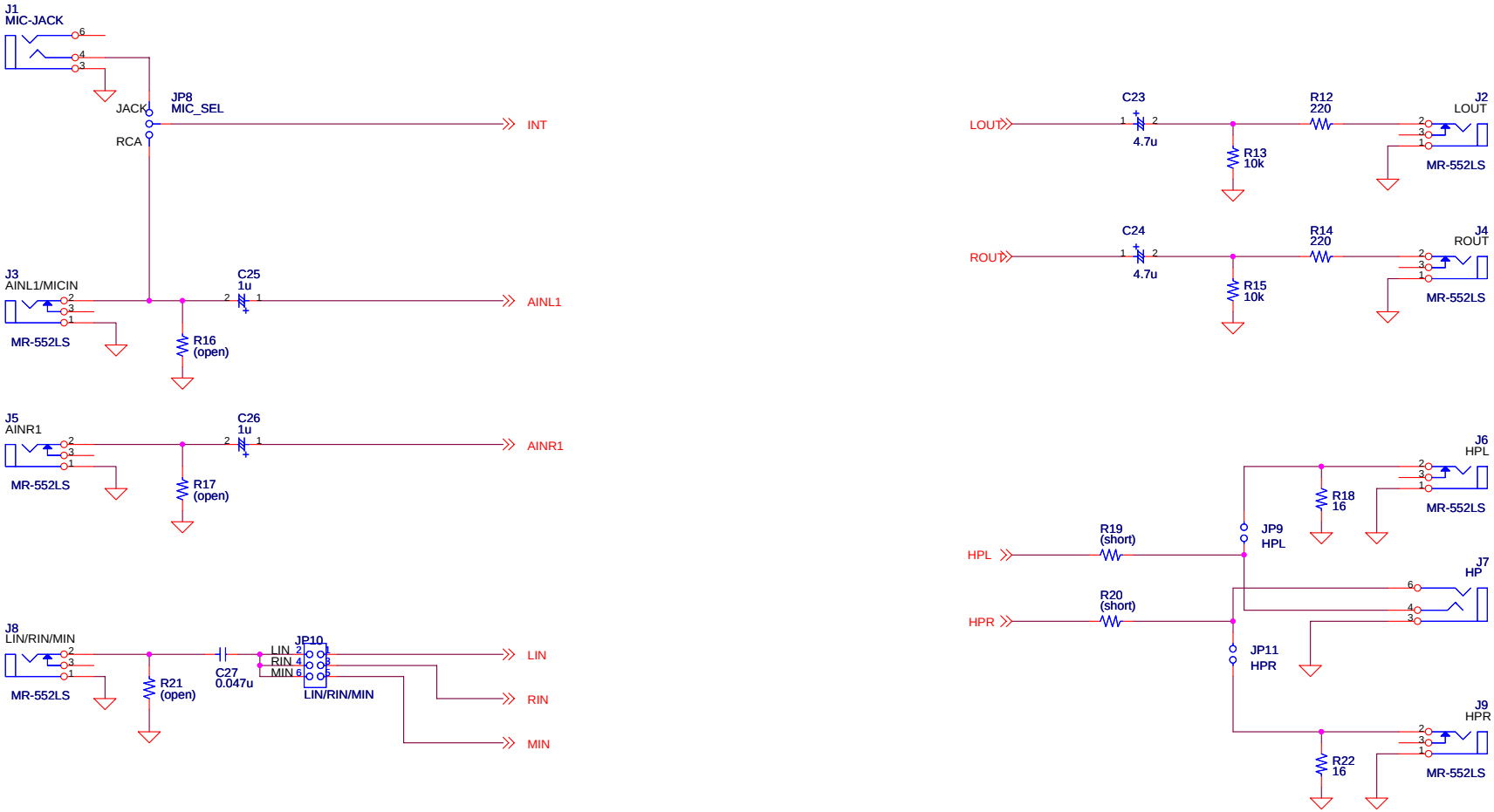
Size: A3	Document Number: AK4665A	Rev: 1
Date: Wednesday, May 17, 2006	Sheet 1 of 4	



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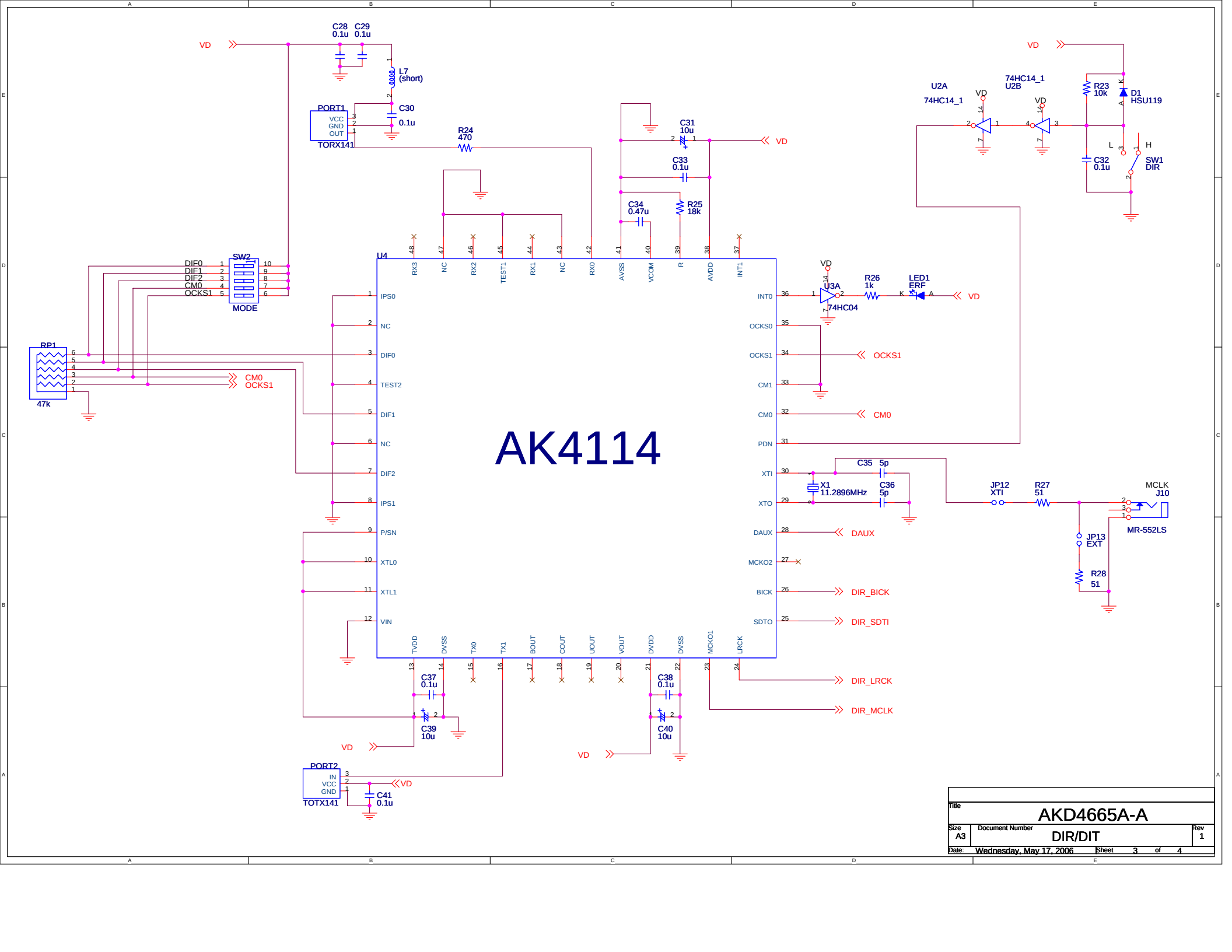
Size: A3	Document Number: ANALOG	Rev: 1
Date: Wednesday, May 17, 2006	Sheet 2 of 4	


AK4114
U4
C28 0.1u
C29 0.1u
L7 (short)
C30 0.1u
PORT1
TORX141
R24 470
C31 10u
C33 0.1u
C34 0.47u
R25 18k
SW2
MODE
DIF0
DIF1
DIF2
CM0
OCKS1
RP1
47k
IPS0
NC
DIF0
TEST2
DIF1
NC
DIF2
IPS1
P/SN
XTL0
XTL1
VIN
RX3
NC
RX2
TEST1
RX1
NC
RX0
AVSS
VCOM
R
AVDD
INT1
INT0
OCKS0
OCKS1
CM1
CM0
PDN
XTI
XTO
DAUX
MCKO2
BICK
SDTO
TVDD
DVSS
TX0
TX1
BOUT
COUT
UOUT
VOUT
DVDD
DVSS
MCKO1
LRCK
U3A
74HC04
R26 1k
LED1 ERF
U2A
74HC14_1
74HC14_1 U2B
R23 10k
D1 HSU119
C32 0.1u
SW1 DIR
L
H
C35 5p
X1 11.2896MHz
C36 5p
JP12 XTI
R27 51
JP13 EXT
R28 51
MCLK
J10
MR-552LS
DIR_BICK
DIR_SDTI
DIR_LRCK
DIR_MCLK
C37 0.1u
C39 10u
C38 0.1u
C40 10u
PORT2
TOTX141
C41 0.1u
VD
Title
AKD4665A-A
Size
A3
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Rev
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Date:
Wednesday, May 17, 2006
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3
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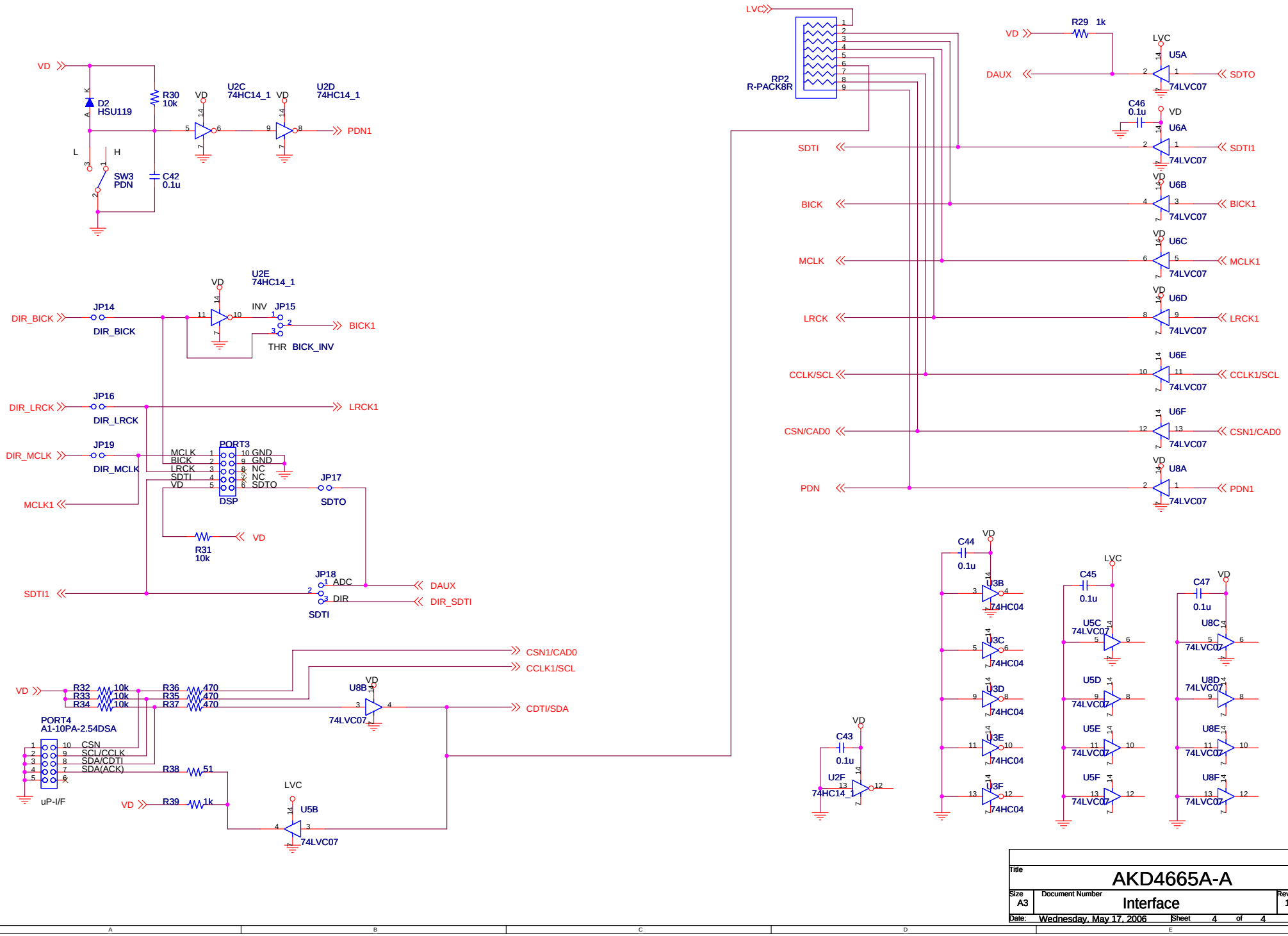
4



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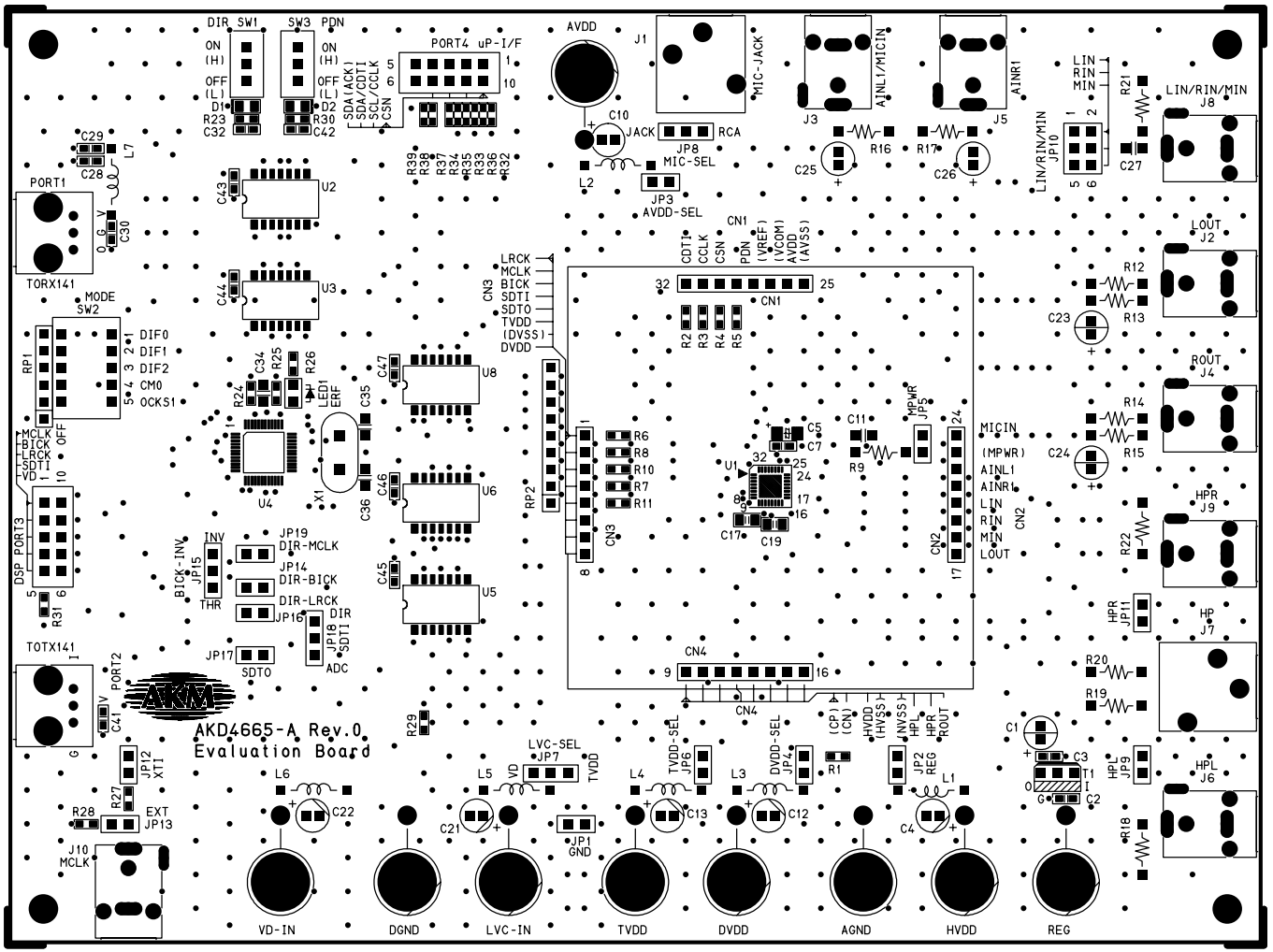
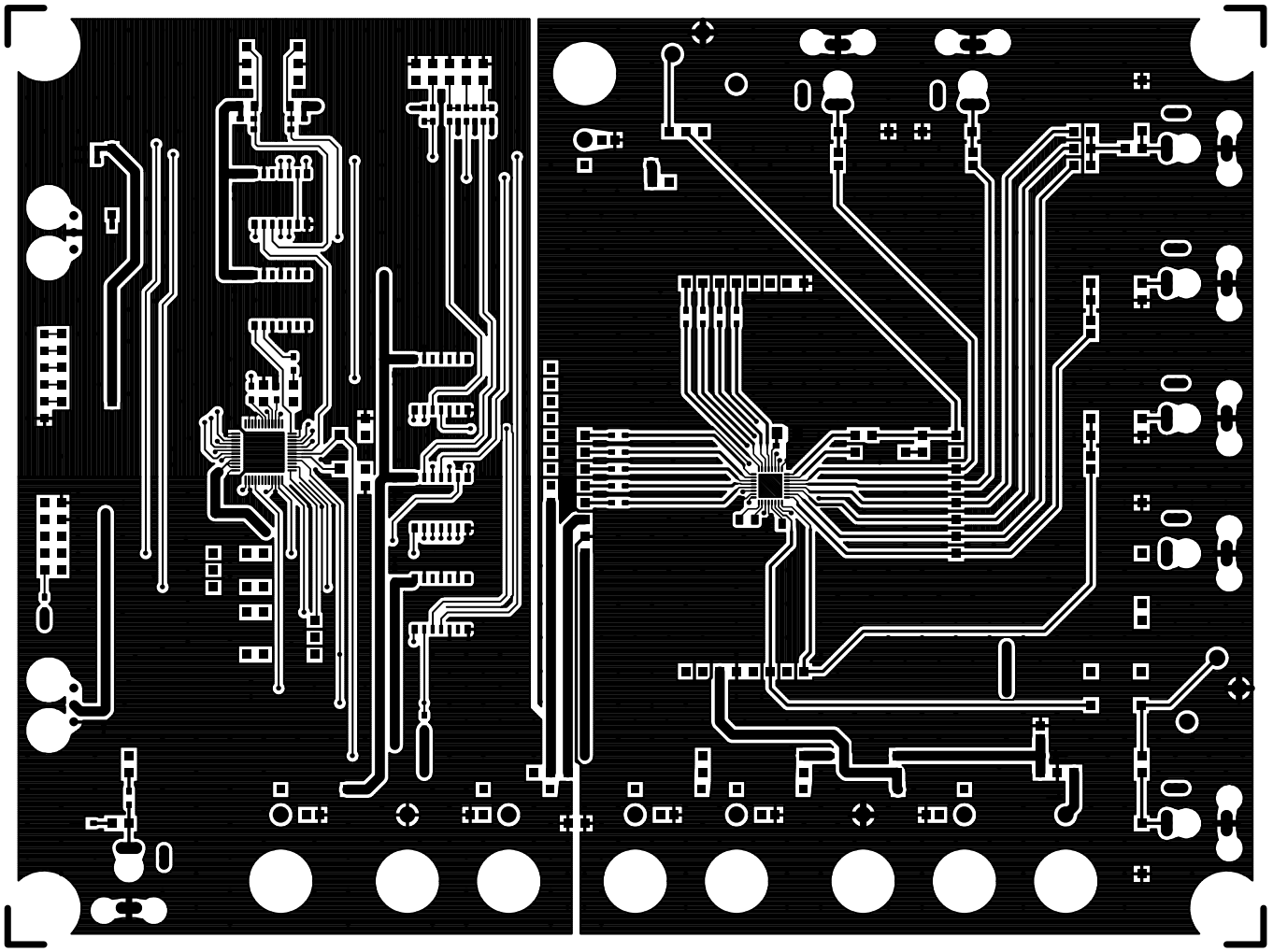
Date: Wednesday, May 17, 2006	Sheet 4 of 4	



AKD4665-A L1 SILK

AKD4665-A L2 SILK



AKD4665-A L1

AKD4665-A L2